

Re: Bowden's BCD clock circuit

Source: <http://sci.tech--archive.net/Archive/sci.electronics.basics/2007-04/msg00503.html>

- *From:* John Popelish <jpopelish@xxxxxxxx>
 - *Date:* Wed, 11 Apr 2007 22:28:18 -0300
-

Greg wrote:

I've decided to build a BCD clock and after searching for a circuit I've decided on Bill Bowden's circuit.

http://ourworld.compuserve.com/homepages/Bill_Bowden/clock.htm

After examining the circuit, though, I'm curious about the circuit giving a pulse every second. There are two NAND gates attached to the 4040 binary counter which then feed into an OR gate. Am I correct in assuming that they should be feeding into AND gate to get a pulse every second? As the circuit stands, I would think it's going to give a pulse on 0.8 sec and on 0.2 sec, or two pulses per second.

I'm fairly weak on logic circuits so forgive the stupid question.

I'll take a shot.

The CD4040 is a binary counter that resets to all zeros out with Q1 being the 1 bit, Q2 being the 2 bit, Q3 being the 4 bit, etc.

<http://www.fairchildsemi.com/ds/CD/CD4040BC.pdf>

The bottom NAND outputs a low when both inputs are high, and these inputs are the 4 and 8 bits.

The upper NAND gate outputs a low when its two inputs are high, and these bits are the 16 and 32 bits.

So starting at a reset, the first count that produces a low from both gates at the same time happens at count $32+16+8+4=60$. This low state is slightly delayed by an RC filter and inverted to a high by the inverter. This rise from low to high clocks the second counter every 60th line cycle and also resets the counter back to zero before the 61st cycle occurs, so when it does, it is counted as 1 of the next 60.

The duration of the second pulse is set by the time delay between when the reset pulse is sent to the counter and how long it takes for the disappearance of the 60 decode passing through the RC filter. That is roughly a millisecond.

.