

## Re: DDR SDRAM with Xilinx Virtex 2 on self designed PCB

**Source:** <http://sci.tech-archive.net/Archive/sci.electronics.cad/2004-11/0317.html>

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**Date:** 11/22/04

Date: Mon, 22 Nov 2004 23:38:42 +1100

On Mon, 22 Nov 2004 13:08:51 +0100, "Elmo"  
<[ikeepthespiritalive@freenet.de](mailto:ikeepthespiritalive@freenet.de)> wrote:

>Hello,

>

>*last week I started the development and design of a PCB with an FPGA (Xilinx  
>Virtex 2) and two DDR-SDRAMs in parallel. No big deal, I thought, keeping in  
>mind the most obvious design rules, i.e. combining the address lines and  
>separating the data and strobe (DQS) lines. But now I came across the many  
>other signals there are, e.g. the clock signals, S0 and S1, CAS, RAS, WE,  
>etc. My first idea was to also combine them for both modules. Lately I  
>wondered if I am right with that assumption?*

>*From the P.O.V. of functionality, that depends on what you want to do.  
Will you need to write to individual bytes? Will you want to be able  
to precharge (or whatever) one of the chips while you are performing a  
different operation on the other chip?*

Signal integrity implications of pairs of SDRAMs (DIMMs, actually) are  
discussed in this recent c.a.f thread:

<http://groups.google.com/groups?threadm=cm7ebv%243e3%241%40news.cs.tu-berlin.de>

Regards,  
Allan