

Re: Power-On Reset

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On Tue, 22 Feb 2005 10:40:56 GMT, Rich Grise <richgrise@example.net> wrote:

>On Tue, 22 Feb 2005 04:10:28 +0000, Paul Rako wrote:

>

>> *POR circuits are NOT trivial to design. Many people
>> have crashed and burned using latches, 555 timers and
>> other schemes. This is why Maxim can get 50 cents for
>> a reset chip. I have been told by very smart people that
>> the only valid approach to a POR circuit is a transistor-
>> level approach. You have to have fully characterized
>> transistor models if you expect to SPICE it, macromodels
>> will not do. Be sure to exercise the circuit (reality preferred
>> to SPICE) for very slow as well as very fast power turn-on and
>> over a range of temperatures and loads. This is really a
>> design challenge so don't take it lightly.*

>

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>What's wrong with a 1 uF cap from the POR pin to ground, with,
>say, a 10K pullup?

Rich, I am unable to tell whether you were being sarcastic, or whether you really don't know why an RC circuit is a bad reset generator (in general).

Commonly encountered supply waveforms that don't produce a reliable reset from the RC circuit:

1. A brief dip in the supply voltage that goes low enough to crash the processor, but it doesn't discharge the cap enough to cause a reset when the supply returns to normal.
2. Very slow dv/dt. The RC circuit will not assert reset.
3. The supply voltage sitting in a "brownout" state indefinitely. The RC circuit will not assert reset.

A good reset generator will hold reset active for all values of supply voltage below some threshold all the way down to zero volts, regardless of dv/dt (except maybe for glitch filtering), and keep reset active for a certain period (some tens to hundreds of ms) after the voltage goes above the threshold.

Regards,
Allan