

Re: Wanted: LM-709 (Spice model) National Op-Amp

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- *From:* Paul Rako <sp_a_mpa_u_1@xxxxxxxxx>
 - *Date:* Mon, 26 Sep 2005 00:48:35 GMT
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Well, let me explain why I decide what package to use based on the layout package. I spent 25 years as a contractor/consultant. The recent rate I charged was 80 to 100 dollars an hour. Believe me, a client does not care about SPICE runs. He wants to see hardware, little green boards. Only then does his blood-pressure drop. As far as they are concerned even drawing a schematic seems silly as well as the layout software. Maybe that is why so very many companies seem to lose the schematic and layout files and want me to improve or fix things with only a Gerber. Then it is off to Protel (or some other package I tend not to enjoy) because it can import a Gerber to the layout package and at least lets you wing things from there.

Now in my mind the most important principle about ECAD is connectivity. That what you draw on the schematic will show up as a flight line in the rats nest and that any gate swaps or re-annotation done in layout can be back-annotated. Having a separate SPICE schematic violates this principle. Now you have something whose coherence is only assured by human inspection.

Now I sure do appreciate the difficulty in making SPICE sources in a schematic for layout or alternatively, connector parts for something that will be SPICEed. And Jim, I think when people talk about the misery of using SPICE Orcad Capture it is the "occurrences" vs "instances" issues I mentioned. You are one of several hard-core designers I have met that prefers PSPICE schematics to capture. There are enough of you that Cadence still lets you download the PSPICE capture program even for 10.5 release.

As to getting the board parasitics back, then you have to leave the lumped element SPICE world and go to 2 or 3-D field solvers like hyperlynx. This is generally referred to as signal integrity. High-zoot hyperlynx that can handle lossy transmission lines is 48 grand or so. And good old Orcad has a hyperlynx output export, even though Hyperlynx is now a Mentor tool.

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Judging our test is just observing the schematic and what one has to do to get good results. Pretty much just read the thread when you get around to it and comment on the methodology and results. We want to enter a schematic Jim Williams built many years ago and see how various SPICE packages do. I also have some PSPICE stuff that did not converge and will post that and bear the withering criticism that I did something stupid or had a bad model. But the group has to understand it is not just about convergence-- it is about having the real board agree with the SPICE results.

Paul

Jim Thompson wrote:

On Sun, 25 Sep 2005 10:17:33 GMT, Paul Rako <sp_a_mpa_u_l@xxxxxxxxxx> wrote:

[snip]

Mr. (Dr./Prof?) Thompson:

"Mr.", I only have a MSEE.

What do you use? I hope it is not some proprietary thing like Analog Devices' internal SPICE.

I use PSpice A/D v10.5, although I'm trying to make time to evaluate a newcomer, TTSpiceWorks <<http://www.trabucotechnologies.com/>>. But it seems, the older I get the busier I get ;-)

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I hope you will serve as
judge jury and executioner in our little test.

What "little test" is it? I haven't been following this thread
closely.

And remember
everyone-- in my opinion we are mis-applying SPICE. The
acronym stands for "Simulation Program with Integrated
Circuit Emphasis" It is not SPBLE. Spible would be
"Simulation Program with Board-Level Emphasis".

Indeed.

This is
why there seems to be such passions aroused when us board
guys say we don't worship SPICE the way IC designers do.

In the IC world we "back-annotate" to add the strays that result from
layout. Do "board guys" have such a tool?

BTW, Dave Tamura in the CAD department at National rolled his
eyes when I told him I said Process and Modeling departments
cost 5 or 10 million dollars a year for a big semiconductor
company. He hinted that tens times those numbers is not
unheard of. He also said that his CAD department is also
involved in making sure the models conform to reality.

[snip]

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And Win wonders why discrete MOSFET models are inadequate ;-)

...Jim Thompson