

## Re: Phase frequency detector

**Source:** <http://sci.tech-archive.net/Archive/sci.electronics.design/2004-06/1749.html>

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**From:** Mike Monett ([mrmonett\\_at\\_yahoo.com](mailto:mrmonett_at_yahoo.com))

**Date:** 06/12/04

Date: 11 Jun 2004 20:50:06 -0700

Mike <[mike@nosпам.com](mailto:mike@nosпам.com)> wrote in message news:<1a95aekr5j4sh\$.1ikvkifedtcnb\$.dlg@40tude.net>...

> On Tue, 8 Jun 2004 07:17:15 -0700, Mike wrote:

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>> On 7 Jun 2004 03:36:53 -0700, Mike Monett wrote:

>>> Mike, I'm having difficulty following your description. Do you  
>>> have a schematic and timing diagrams, perhaps a SPICE model?

> Here's a Python program that does the calculations and reports the  
> results.

Mike, thanks for posting the code. I'm not familiar with Python but it seems clear and readable enough.

Also, I want to thank you for the very useful information you have posted on phase noise, and for the numerous links you have provided in your various postings. In particular, the ones by Lee and Hajimiri on Oscillator Phase Noise were very useful and I had not come across them before. And, thank you for the very important prior art info you found on the Binary Sampler – that was very helpful.

The reason I mention this is I find your posts valuable, and don't want you to think I am attacking you in any way. I've been thinking about the problem of how a seemingly reliable pll can suddenly experience 100% failure, and have come to some conclusions that may differ from yours.

First, the mode of failure is very strange. How can a simple pfd work in different applications for years, then suddenly go bad?

It doesn't seem possible that it can be caused by one of the latches resetting too quickly, leaving the other one still active. The set and reset are one of the fastest circuits in D-flops, and the minimum pulse widths are among the shortest listed in the datasheet.

Also, as Camenzind shows in Chapter 5, the first principle of linear design is to rely on the close matching of parameters in semiconductors. (Thanks for the url, Jim)

<http://www.arraydesign.com/download/CHPTR5.PDF>

This means both flops should have similar reset times. When the feedback path includes the prop delay of an added gate, the resulting reset pulse width seems more than sufficient to guarantee that both flops or latches will be reset.

Recall this circuit has been used for decades and millions of parts have been shipped without problem. So why should it suddenly show up in your product? If there were problems in resetting the latches, it should have been there from the beginning.

One indication of the true problem might be that your code doesn't seem to account for the prop delay and risetimes of the current sources. In fact, it appears your code can produce no result other than a straight line, regardless of how much deadband is actually present in the circuit!

Perhaps this kind of analysis really needs to be done in SPICE, which can do a better job handling the transients involved. An example is shown in Fig. 6 of Johansson's "A Simple Precharged CMOS Phase Frequency Detector", IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998. (Please Note – I do not necessarily agree with anything else he says, but the SPICE simulations are nice:)

<http://iroi.seu.edu.cn/jssc9899/33ssc98/33ssc02/pdf/33ssc02-johansson2.pdf>

So I think your code misled you into believing that deadband was impossible in your circuit. Also, from your response, it appears you do not have a dedicated tester to view the response of the pll to a variable pulse. Without this simple test, you have no way to look at the response of the latches and charge pumps and see how much margin actually exists before deadband sets in.

Now here's my hypothesis. You had a small amount of deadband in your circuit from the beginning, but with your typical use, it never showed up. Perhaps the normal system jitter was sufficient to mask the deadband.

However, the new customer required a faster lock time, which means increased loop bandwidth. Perhaps the system noise was also better, which gave reduced system jitter. Under the new conditions, the loop developed a limit cycle oscillation, which can grow to be quite large.

This may have misled you into believing there was a problem resetting the latches. So you installed Jim's DualD-PFD circuit and the problem went away:

<http://www.analog-innovations.com/SED/DualD-PFD.pdf>

It is true his circuit works as you have described. It is also true that it adds two prop delays to the reset path, which increases the time that both current pumps are turned on in each cycle. If this exceeds the risetime of the current pumps, the deadband disappears. I am confident if you remove Jim's circuit and simply add an equivalent delay in the reset path, you will obtain a similar result.

Does this hypothesis sound reasonable and does it fit the available information?

Best Wishes

Mike