

Re: MOSFET help?

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Stefan Heinzmann wrote...

>
> *Ed ed-at-micra-org-uk wrote:*
>
>> *Hi All possibly quite a simple question but I would like some advice.*
>>
>> *I have been looking at ways to use an IRFZ44N as a solid state 'switch'*
>> *to switch on and of the positive supply of a 12 to 24 volt supply. As*
>> *far as current requirements go the IRFZ44 is ideal, but I'm sturrgling*
>> *to find a good way to do this. [snip comment] To fill in more info*
>> *its for a high current serial bus of 3 wires, 12-30v Ground and Data.*
>>
>> *I need to beable to control the Data and Supply lines from a 5 volt*
>> *logic level as simply and as ruggidly as possible, yet both must be*
>> *capable of high currents, and minimal on resistance. I looked at using*
>> *a P channel fet, such as the IRF5210 thinking this may be a solution,*
>> *but I think I am going totally the wrong way.*
>
> *Using a P-channel MOSFET does indeed simplify things considerably, as*
> *your gate drive voltage needs to be lower than the source voltage. It*
> *still can not be driven directly from a logic output as the logic levels*
> *are grond referenced whereas the MOSFET doesn't see any ground voltage.*
>
> *So my recommendation would be to use a P-channel MOSFET together with a*
> *level-shifter between the logic output and the MOSFET gate. This level*
> *shifter can be as simple as a transistor (NPN) and a couple of resistors.*
>
> *Here's a sketch of the idea (to be read using a monospace font):*
>
> *MOSFET*
>
> *Power in -----o-----+^+----- Switched power out*
> *| |||*
> *| ===*
> *| R1 |*
> *| ___|*
> *+ -|___| - -o*
> *|*

```

> /
> ___//
> Control signal-----/___/----/ NPN
> />
> R2 /
> /
> ===
> GND
>
> R1 ensures that the MOSFET turns off when the NPN turns off. Its value
> should be low enough to make the MOSFET switch off quickly enough and
> high enough not to exceed the NPN's ratings. R2 limits the base current
> of the NPN.

```

This configuration may be useful for switching fixed low-voltage power supplies, but if the supply voltage is above 15 to 20V, the FET's rated gate voltage will be exceeded. Furthermore, the gate voltage is not predictable. A good general purpose configuration is to develop fixed p-channel FET gate voltages by switching fixed currents into the gate resistor, like this:

```

| p-type FET
| Power in -----o-----, ,----- Switched power out
| 15 - 50V | S_|_|_|
| (65V max) | ,----
| |
| '- R1 --+ for 10V gate drive, use
| 1.0k | R1 = R2 (10/4.3) = 2.3 R2
| |
| |
| |
| 5V logic-control -----| 60V NPN BJT
| |V 2n4401
| |
| R2 level-shift current-sink
| 430 high-side FET switching
| |
| GND

```

The fixed gate drive current of this configuration means that it's easy to add a current-limit feature, unlike the simple CE switch.

```

| p-type FET
| Power in ---o--- Rs ---+-----, ,----- Switched power out
| 15 - 50V || S_|_|_|
| (65V max) | 2n4403_|_| ,---- current limit
| |_____|>/\_____| I_cl = 0.65 / Rs
| |
| |
| '------ R1 -----+
| 1.0k |
| |
| |
| |

```

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```
| 5V logic-control -----| 60V NPN BJT
| \|V 2n4401
| |
| R2
| 430 ohms
| |
| GND
```

Actually, it's a wise idea to use foldback current limiting to reduce the C.L. dissipation for the FET. Although this takes only two more parts (as we show in AoE), two parts are time costly in s.e.d. ASCII drawings, and one's intrinsic laziness prevails.

Thanks,
- Win

(email: use hill_at_rowland-dot-org for now)