

Re: Crystal drift

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Phil Hobbs <pcdhSpamMeSenseless@us.ibm.com> wrote

>> *Mike Monett wrote:*

>>> *Sideband locking is a possible strategy here. If you mix the two
>>> oscillators together, you can phaselock the beat note to a
>>> function generator with a frequency-phase detector, e.g. a
>>> 4046--it won't lock up to the image frequency, because the sign
>>> of the loop gain is opposite for the two sidebands.*

>> *Wouldn't the pll rail if it approached the image from the wrong
>> direction?*

> *It won't rail [...]*

Sure it will. Consider a lower sideband system with a reference signal at 10 MHz, a vco at 9,999,999 Hz, and a pfd at 1 Hz.

Case 1: If the vco frequency decreases, the difference frequency between the reference and the vco increases. Therefore the pll must increase the vco frequency to regain lock.

Case 2: If the vco frequency goes above the 1 Hz target, the difference will decrease, and the pll must decrease the vco frequency to regain lock.

If the vco frequency is well above the reference, say at 10,001,000 Hz, the difference is greater than the 1 Hz target. This will cause the vco frequency to increase as in Case 1. However, it is already too high and the loop will rail.

If the vco is above the reference, but below the 1 Hz target, the difference is below 1 Hz and the pll will decrease the vco frequency as in Case 2. The mixer output goes to zero when the vco is equal to the reference, and the pll output will decrease the vco frequency as before. The vco will then cross the reference and lock on the proper point.

So it is important to approach lock from the correct direction.

>>> *By making the loop narrow enough, you can avoid having the beat
>>> note modulate the VCXO significantly.*

>> *Aren't you locking to the beat frequency? With a phase/frequency
>> detector and a balanced charge pump that has zero deadband, there
>> should be very little ripple on the output.*

> *Yes, but not *none*. This is an ultraprecise application, after
> all.*

We are talking about very low offset frequencies. Any reference spurs on the vco will be buried in the close-in phase noise.

[...]

>> *Also, depending on the frequency, a simple D-flop makes an
>> excellent digital mixer. Put one input on the clock, the other on
>> the D. The Q output will switch at the difference frequency.*

> *Not with a PFD--metastability will blow you right out of the
> water. Every lost cycle equals lost lock.*

Definitely not true. A missing or extra transition will have little or no effect in a narrowband loop since it won't have time to move far. The clocks will remain within the feedback reset time and the problem will get corrected on the next cycle.

The biggest problem with the digital mixer is multiple transitions at low offset frequencies due to phase jitter.

For example, the time delta between samples is

$$\text{Offset Delta} = \frac{\text{Offset}}{F_s^2}$$

where

Offset = Offset Frequency in Hz
Fs = Signal Frequency in Hz

A 1 Hz offset at 10 MHz gives a time delta of $1 / 1e14 = 10$ fs. So every 100 ns, the sampling point moves over 10 fs. Since most signals have rms jitter values much higher than this, the digital mixer will produce a string of random transitions as the phase goes through zero. This will mess up a pfd or any trigger circuit. The solution is to fire a single-shot on the first transition and ignore the rest.

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The Binary Sampler test circuit uses a single shot on the output of the digital mixer in Fig. 1, but it is not shown due to lack of space:

<http://www3.sympatico.ca/add.automation/sampler/design.htm>

> *Cheers,*

> *Phil Hobbs*

Mike Monett