

Re: Timer circuit help

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2004-11/5809.html>

From: Fred Bloggs (*nospam_at_nospam.com*)

Date: 11/23/04

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Terry Pinnell wrote:

> *kensmith@green.rahul.net (Ken Smith) wrote:*

>

>

>>> *Neat, _and_ 50% duty cycle, but since the earliest output from the
>>>4060 is Q3, there will be 8 clock cycles between IN going high and OUT
>>>going active, which isn't what the OP's timing diagram:*

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>>

>>*No, the circuit works fine. Those are all NOR gates.*

>>

>>*When the reset first goes away, Qn is low. The output goes high right
>>away.*

>>

>>*After some clock cycles, Qn goes high causing the low on the output.*

>>

>>*After that same number of pulses, Qn goes low.*

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>>

>>>*Input:*

>>> _____

>>> ____/ |__.....

>>>

>>>*Output:*

>>> _ _ _____

>>> ____/ |_/ |_/ |__.....

>>>

>>> ^ 3-4 pulses 50% duty cycle ~6 Hz

>>>

>>

>

> *I'd hoped to breadboard your neat solution but found I had no 4060s.*

> *And when I turned to CircuitMaker to try a simulation instead, I was*

> *disappointed to find its model library has no 4060.*

- >
- > *However, it does have the 4020, which is essentially an almost*
- > *identical 14-stage ripple counter, although lacking the oscillator*
- > *section of the 4060. But so far my attempts to implement your approach*
- > *with a 4020 (and a few NORs, which I assume are 4001s?) has failed.*
- > *Anyone else able to do that please?*
- >

You don't need any NOR gates whatsoever– you take Q_{n+3} and stuff a one on that RTC input of the oscillator, pin 10, through a diode and the 4060 freezes in $Q_n=0$ state which is the turn-on polarity for the bulb. The n runs 1–14 and then $RT \times CT = 1/(2.3 \times 6\text{Hz} \times 2^n)$ by the data sheet.