

Re: Timer circuit help

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From: Fred Bloggs (*nospam_at_nospam.com*)

Date: 11/23/04

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Fred Bloggs wrote:

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> *Terry Pinnell wrote:*

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>> *kensmith@green.rahul.net (Ken Smith) wrote:*

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>>

>>>> *Neat, _and_ 50% duty cycle, but since the earliest output from the
>>>> 4060 is Q3, there will be 8 clock cycles between IN going high and OUT
>>>> going active, which isn't what the OP's timing diagram:*

>>>

>>>

>>>

>>> *No, the circuit works fine. Those are all NOR gates.*

>>>

>>> *When the reset first goes away, Qn is low. The output goes high
>>> right away.*

>>> *After some clock cycles, Qn goes high causing the low on the output.*

>>> *After that same number of pulses, Qn goes low.*

>>>

>>>

>>>

>>>

>>>

>>>> *Input:*

>>>> _____

>>>> ____/|____.....

>>>>

>>>> *Output:*

>>>> _ _ _____

>>>> ____/|_|_||____.....

>>>>

>>>> ^ 3-4 pulses 50% duty cycle ~6 Hz

>>>>

>>>

>>

sci.electronics.design: Re: Timer circuit help

>> *I'd hoped to breadboard your neat solution but found I had no 4060s.*
>> *And when I turned to CircuitMaker to try a simulation instead, I was*
>> *disappointed to find its model library has no 4060.*
>>
>> *However, it does have the 4020, which is essentially an almost*
>