

Re: PCB Power Trace Widths, Ground Planes, and Routing

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Thank you for your informative replies.

I'm using a two layer board since it is \$33 at www.33each.com with the student discount. I suppose I could go to a four layer board. How much more do these usually run? (The price isn't listed on 33each.com. I need to call for a quote.)

What speed qualifies as high speed? Which buses qualify as highly active buses? The ARM is able to be clocked up to 66MHz, but I'm running it at 20MHz (4x 5MHz osc. via PLL) to avoid much these high speed effects. The ethernet section is running at 20MHz as well, but off a separate crystal to allow me to clock the ARM faster, independently of the CS8900. The TI Codec is running at 2.048MHz of another osc. The ARM has an 18-bits of the address bus running to SRAM, 1-bit to the LCD controller, and 3-bits to the CS8900. The 16-bit data bus runs 16-bits to SRAM and the CS8900, and 8-bits to the TI Codec and LCD Controller. During development, SRAM will hold program code and be frequently accessed. The TI Codec and CS8900 will be the other two frequently accessed chips (VoIP application).

Should I make separate analog ground planes for the TI Codec and CS8900? Why do the chips have separate analog and digital grounds (AVss and DVss)? Can I connect these to one ground plane? If to separate ground planes, how should the planes connect to ground.

The 5V is to power an onboard LCD the CPLD LCD controller. The 2.5V is the supply for the ARM core. The rest of the system is 3.3V. So I should make the power plane 3.3V and run 100 mil traces in the same layer (maybe around the edges?) for the other two supplies? How can I tell the auto-router to make the trace smaller as it gets closer to the SMT chips? Currently the auto-router tries to run 100mil traces straight to the SMT pins and looks like it shorts them, though that could simply be a visual effect. I'm using Protel DXP.

Since this is a student project, I don't need to meet FCC testing. If you're interested in the class, here is the website:

sci.electronics.design: Re: PCB Power Trace Widths, Ground Planes, and Routing

<http://wolverine.caltech.edu/eecs53/>

Cheers,
Chris