

Re: PCB Power Trace Widths, Ground Planes, and Routing

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On Sat, 25 Dec 2004 19:23:09 -0800, Apparatus wrote:

- > Thank you for your informative replies.
- >
- > I'm using a two layer board since it is \$33 at www.33each.com with the
- > student discount. I suppose I could go to a four layer board. How much
- > more do these usually run? (The price isn't listed on 33each.com. I
- > need to call for a quote.)

Check pcbexpress.com, too.

If you don't mind using their free software, you can also use [expresspcb](http://expresspcb.com). They are reliable, but a lot of people don't like using them because their software uses special output formats that aren't compatible with other vendors.

- >
- > What speed qualifies as high speed? Which buses qualify as highly
- > active buses? The ARM is able to be clocked up to 66MHz, but I'm
- > running it at 20MHz (4x 5MHz osc. via PLL) to avoid much these high
- > speed effects. The ethernet section is running at 20MHz as well, but
- > off a separate crystal to allow me to clock the ARM faster,
- > independently of the CS8900. The TI Codec is running at 2.048MHz of
- > another osc. The ARM has an 18-bits of the address bus running to SRAM,
- > 1-bit to the LCD controller, and 3-bits to the CS8900. The 16-bit data
- > bus runs 16-bits to SRAM and the CS8900, and 8-bits to the TI Codec and
- > LCD Controller. During development, SRAM will hold program code and be
- > frequently accessed. The TI Codec and CS8900 will be the other two
- > frequently accessed chips (VoIP application).

All continuous clocks are high speed, no matter how fast they are. Any bus that runs continuously should be treated as high speed. This includes all RAM, etc. And, as John Larkin said, the edge rate of the signal can make it fast, even if the clock rate isn't. I would say all of your buses are probably high speed. An example of a non-high-speed bus would be the SMBus serial bus on Intel architecture systems.

Here is a little tip for you. The clocks on digital boards cause 90 percent of signal integrity and RF interference problems. So leave good clearance around the clock traces (this helps keep them from adding noise to other signals), and try to avoid changing reference plane when you route them. That is, if they are next to a ground layer, keep them next to ground layers. Don't switch to a VCC layer. And if they are next to a VCC layer, keep them there. This helps keep them from emitting RF. At my previous job, our standard procedure was to put series resistors near all clock sources, and shunt capacitors near all clock loads. This allows you to control the edge rate to keep RF emissions down, and you can slightly tweak the signal delay if you find you have a skew problem. Often the resistor would be replaced with a "jumper", and the capacitor would not be populated. But this is preferable to redesigning the board to incorporate them if they are needed. Also, avoid routing other signals near the clock generator, buffer, and multiplier chips. They are infamous for coupling noise to other signals.

- >
- > *Should I make separate analog ground planes for the TI Codec and CS8900?*
- > *Why do the chips have separate analog and digital grounds (AVss and DVss)? Can I connect these to one ground plane? If to separate ground planes, how should the planes connect to ground.*

Splitting ground planes is problematic because, as I said, you shouldn't route signals across the split on layers adjacent to the plane, and usually, you have to. So it is better to stick to one ground plane, and decouple it appropriately.

I usually filter the AVDD with series inductor and several shunt capacitors (to ground) of different values and package sizes. I have never tried not doing this, but I have had good luck so far with this approach.

- >
- > *The 5V is to power an onboard LCD the CPLD LCD controller. The 2.5V is the supply for the ARM core. The rest of the system is 3.3V. So I should make the power plane 3.3V and run 100 mil traces in the same layer (maybe around the edges?) for the other two supplies? How can I tell the auto-router to make the trace smaller as it gets closer to the SMT chips? Currently the auto-router tries to run 100mil traces straight to the SMT pins and looks like it shorts them, though that could simply be a visual effect. I'm using Protel DXP.*

I've never used an auto-router. Usually other people have manually routed my boards for me, according to my instructions. Maybe you could route some of the critical nets manually first, and then submit the job to the auto-router?

The idea I have in mind for you is to not route traces on the power plane at all. Instead, I am imagining that you will have a VCC plane that will mostly be 3.3V, but with an island of 5 V near the LCD and CPLD, and island of 2.5 near the ARM (unless it uses both 2.5 and 3.3.

Does it?). Connect the 5V and 2.5V supplies to the islands using wide traces. I imagine 100 mils would be fine. Be sure to use multiple vias.

If the arm has 3.3V for the I/O supplies, you may find that the 3.3 V and the 2.5 V are spacially segregated. In BGA's, the innermost area is often the core voltage with the IO voltages in the outer balls. I don't know if your ARM chip is like this or not. If it is, try to make an island that captures all the 2.5V pins or balls, including decoupling caps, but make it as small as you can, and try to keep it away from 3.3V pins or balls if you can.

Usually, I don't decide how to cut up the power plane until after I place most of the parts on the board. Then I set the different voltages to different colors and try to visualize where the different islands should go. Sometimes it is hard. Sometimes it is easy. Sometimes you just have to do the best you can and hope it works. I try to keep the islands rectangular, or at most slightly pan-handled. It is OK to have multiple islands of the same voltage, as long as they are connected by fat traces. Your 100 mils would be plenty, I think. The individual islands should be decoupled to ground just as if they were continuous planes.

>

> *Since this is a student project, I don't need to meet FCC testing.*

Good. That makes the job a lot easier.

> *If*

> *you're interested in the class, here is the website:*

> <http://wolverine.caltech.edu/eecs53/>

>

> *Cheers,*

> *Chris*

Good luck! Stay on top of it and try to get things done early. This is a fairly big task if you've never done it before!

—Mac