

## Re: Is microprocessor an integrated circuit???

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**From:** Thaas ([mysig\\_at\\_sprynet.com](mailto:mysig_at_sprynet.com))

**Date:** 01/29/05

Date: Sat, 29 Jan 2005 20:11:55 GMT

On Sat, 29 Jan 2005 10:37:28 -0800, John Larkin  
<[jjSNIPlarkin@highTHISlandPLEASEtechnology.XXX](mailto:jjSNIPlarkin@highTHISlandPLEASEtechnology.XXX)> wrote:

>On Thu, 27 Jan 2005 14:18:42 GMT, Thaas <[mysig@sprynet.com](mailto:mysig@sprynet.com)> wrote:

>

>>In the 1970s minicomputers had what are now retroactively defined as  
>>"complex" instructions to perform operations like say allocating a  
>>free page of physical memory to a program's virtual address space. In  
>>the Modcomp IV this was the AMEM instruction. Two other "complex"  
>>instructions in that machine were the MMRB (Move Memory to Register  
>>Block) and MRBM (Move Register Block to Memory).

>>

>

>The VAX had POLY: evaluate a polynomial. Most of the transcendental  
>math functions were microcoded, too.

>

>John

In 1981 Modcomp's president went to a California design firm for the design of their fully 32-bit machine, the 32/85. I remember the section of firmware for the transcendental instructions that were added to that machine were entitled "Transcendental Meditations" by the programmer.

He was in a hurry for the project to end because he was scheduled to attempt Mount Everest that year. Name of Igor Mamadlian IIRC.

Earlier machines implemented the Floating Point instructions on a separate microcoded processor board. The I/O processors were also separate processor boards. The Space Shuttle launch control system uses Modcomp computers with extra customized CPU boards that are used to communicate with other computers in the system through the 64KB Common Data Buffer.

I designed the CPU of Modcomp's 9250, the gate array version of the 32/85 design. Reduced six 14.5" by 19" boards to one. The Instruction Stream Processor was one 55K-gate standard cell. The Memory Management Control used one gate array. The Data Cache Controller was implemented in two identical gate arrays.

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The WCS was implemented in SRAM SIPs as was the register block storage which also held the constants for those transcendentals among other things. All external to the ISP ASIC.

We never called any Modcomp minicomputer or CPU board or even the ISPs of our gate array designs microprocessors. Gee, I guess I should update my resume. According to Bradley I've been designing the damn things for years! Shucks folks! I've designed microprocessors in wire-wrap!

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Thaas