

## Re: Slight digression Re: Power-On Reset

**Source:** <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-02/5222.html>

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**From:** Ken Smith ([kensmith\\_at\\_green.rahul.net](mailto:kensmith_at_green.rahul.net))

**Date:** 02/23/05

Date: Wed, 23 Feb 2005 14:54:49 +0000 (UTC)

In article <bfcol1dv6vasme5v2nro90l22ja5u3el14@4ax.com>, Allan Herriman <[allan.herriman.hates.spam@ctam.com.au.invalid](mailto:allan.herriman.hates.spam@ctam.com.au.invalid)> wrote:  
>On Tue, 22 Feb 2005 19:29:16 +0000 (UTC), [kensmith@green.rahul.net](mailto:kensmith@green.rahul.net)  
>(Ken Smith) wrote:  
[...]  
>>Many FPGA and CPLD circuits do not become sane until the supply voltage  
[...]  
>I fixed it by gating the port outputs with a 74HC part.

Unfortunately I just caught a part holding its output high until Vcc was high enough to be taken as logic high by a 74HC part. I've had to add and gate to the system.

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[kensmith@rahul.net](mailto:kensmith@rahul.net)    forging knowledge