

Re: Current source design (tricky?)

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-03/2181.html>

From: Larry Brasfield (donotspam_larry_brasfield_at_hotmail.com)

Date: 03/12/05

Date: Sat, 12 Mar 2005 12:37:53 -0800

"Fred Bloggs" <nospam@nospam.com> wrote in message
news:42334D1C.8070303@nospam.com...

>

>

> *Larry Brasfield wrote:*

>> *"Fred Bloggs" <nospam@nospam.com> wrote in*

>> *message news:4232DFB9.3020107@nospam.com...*

>>

>>> *Larry Brasfield wrote:*

>>>

>>>> *"Terry Given" <my_name@ieee.org> wrote in message*

>>>> *news:qypYd.8841\$1S4.942601@news.xtra.co.nz...*

>>>>

>>>>> *Larry Brasfield wrote:*

>>>>

>>>>...

>>>>

>>>>>> *A number of op-amps on the market today are*
>>>>>> *very tolerant of capacitive loading because they*
>>>>>> *have a feature whereby that loading causes the*
>>>>>> *gain-bandwidth of the part to drop, almost in*
>>>>>> *proportion to the loading, such that the extra*
>>>>>> *pole remains far enough above the unity gain*
>>>>>> *crossover frequency that stability is preserved.*
>>>>>> *The LM8261 suggested by Mr. Hill is a good*
>>>>>> *example of this class.*

>>>>>

>>>>>> *I have been bitten quite badly by a similar "feature" in*

>>>>>> *the LM6134 (its a slew-rate modification).*

>>>>>

>>>>>> *The feature I mentioned above works by causing the*
>>>>>> *effective value of an internal capacitance to increase.*
>>>>>> *So it changes both the linear small-signal response*
>>>>>> *(less GBW) and the slew limiting (slower).*

>>>>

>>> *Nah- you're full-o-shyte! The capacitive loading decreases the effective internal capacitance due to Miller effects because it*

>>>reduces the gain.

>>

>>

>> You are the one who is full of it, Fred.

>>

>> The way the feature works, typically, is by means of
>> a capacitor placed between the output and the "gain
>> node", the internal node where current sources develop
>> the device's voltage gain. The output buffer, under light
>> load conditions, bootstraps this capacitor so that it does
>> not much load the gain node relative to the AC grounded
>> integrating capacitor. When a capacitive load is present,
>> the increased drop across the buffer output impedance
>> increases the current that must be supplied to the "gain
>> node" for any given dV/dt . This represents an increase
>> in the effective capacitance loading the "gain node", and
>> serves to reduce the gain bandwidth while tending to
>> leave the excess poles unchanged.

>>

>> Miller effect has very little to do with it. In fact, Miller
>> effect, to the small extent it occurs, acts only to slightly
>> move some internal excess pole(s) out a little bit when
>> a capacitive load is present.

>>

>> You, or at least anybody capable of learning something,
>> can see a description of this feature's operation and a
>> schematic in the datasheet for Linear Technology's LT1812.

>> Start at:

>> <http://www.linear.com/pc/productDetail.do?navId=H0.C1.C1154.C1009.C1022.P1838>

>>

>> [More blather founded on spite and ignorance cut.]

>> ...

>>

>>> who has never built anything in his life.

>>

>>

>> Your ability to discern such a falsehood from such a
>> distance with so little evidence marks you.

>>

>

> That's not what the LM8261 is doing– it is Miller effect on two CE output transistors– and that is the OA
you mentioned.

You are exhibiting poor reading skills here, Fred.

What I described above, before another poster
ever mentioned the LM8261, is indeed different
from what the LM8261 does. I never claimed
that the LM8261 acts as I describe above, and,
in fact, I expressly denied in this very thread that
the LM8261 acts per the above.

As for the LM8261 relying on Miller effect, you clearly do not understand the large-signal behavior that is clearly evident from both the description and schematic published in the LM8261 datasheet. To review, (for the benefit of those who are not pig-headed), Miller effect occurs when a voltage gain stage has capacitive feedback into its input, and occurs under small signal conditions as well as large signal conditions. The "capacitive load accomadation" feature described for the LM8261 is strictly limited to large signal conditions. So, how one might confuse it for Miller effect is a puzzle. Care to explain that, Fred? Perhaps you should limit your intellectual exertions to the name calling that you have practised so diligently.

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--Larry Brasfield
email: donotspam_larry_brasfield@hotmail.com
Above views may belong only to me.