

Re: Can PLL Freq Error be zero?

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-03/3195.html>

From: Genome (*ilike_spam_at_yahoo.co.uk*)

Date: 03/17/05

Date: Thu, 17 Mar 2005 22:44:33 GMT

"John Larkin" <jjlarkin@highNOTlandTHIStechnologyPART.com> wrote in message news:jkvj311eeujkg4gu2nqctaqllems2nusmc@4ax.com...

> On Thu, 17 Mar 2005 20:03:50 GMT, "Genome" <ilike_spam@yahoo.co.uk>

> wrote:

>

>>

>> "John Larkin" <jjlarkin@highNOTlandTHIStechnologyPART.com> wrote in message

>>> news:rnmj3195n36dh5cqhcrkimbmjjoef3m2p@4ax.com...

>>> On Thu, 17 Mar 2005 18:44:31 GMT, "Genome" <ilike_spam@yahoo.co.uk>

>>> wrote:

>>>

>>> *But sure, if the divider delay is significant, then it's significant.*

>>>

>>> *Is that better?*

>>>

>>> *John*

>>>

>>>

>>

>> *OK.*

>>

>> *Being thick I miss the meaning of,*

>>

>> $U' = U / S$

>>

>> *and*

>>

>> $W' = W / S$

>>

>> *DNA*

>>

>>

>

> *Oh. I meant that the 'new' VCO frequency (after substituting the black*

> *box) is the old one scaled by the divisor thing, and likewise W' is*

> *the effective new VCO constant (Hz/volt or whatever) after the*

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- > *substitution. It's just like wrapping a dotted line around the*
- > *VCO+divider and replacing the whole mess with a slower, scaled VCO.*
- >
- > *I'm sort of used to a notation where*
- >
- > *G' is the new/scaled/denormalized/fudged value of G*
- >
- > *which is what the filter folks do. But maybe that's not an accepted*
- > *convention.*
- >
- >
- > *John*
- >

Oh, so S is the number by which things are divided, the divisor, and has nothing to do with that Laplace stuff?

DNA