

Re: Can PLL Freq Error be zero?

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-03/3206.html>

From: John Larkin (jjlarkin_at_highNOTlandTHIStechnologyPART.com)

Date: 03/17/05

Date: Thu, 17 Mar 2005 15:18:44 -0800

On Thu, 17 Mar 2005 22:44:33 GMT, "Genome" <ilike_spam@yahoo.co.uk> wrote:

>
> "John Larkin" <jjlarkin@highNOTlandTHIStechnologyPART.com> wrote in message
> news:jkvj311eeujkg4gu2nqctaqdlems2nusmc@4ax.com...
>> On Thu, 17 Mar 2005 20:03:50 GMT, "Genome" <ilike_spam@yahoo.co.uk>
>> wrote:
>>
>> >
>> > "John Larkin" <jjlarkin@highNOTlandTHIStechnologyPART.com> wrote in
> message
>> > news:rnmj3195n36dh5cqhcrgekimbmkjoef3m2p@4ax.com...
>> >> On Thu, 17 Mar 2005 18:44:31 GMT, "Genome" <ilike_spam@yahoo.co.uk>
>> >> wrote:
>> >>
>> >> But sure, if the divider delay is significant, then it's significant.
>> >>
>> >> Is that better?
>> >>
>> >> John
>> >>
>> >>
>> >>
>> >>
>> >OK.
>> >
>> >Being thick I miss the meaning of,
>> >
>> > $U' = U / S$
>> >
>> >and
>> >
>> > $W' = W / S$
>> >
>> >DNA
>> >
>> >
>>

>> *Oh, I meant that the 'new' VCO frequency (after substituting the black
>> box) is the old one scaled by the divisor thing, and likewise W' is
>> the effective new VCO constant (Hz/volt or whatever) after the
>> substitution. It's just like wrapping a dotted line around the
>> VCO+divider and replacing the whole mess with a slower, scaled VCO.
>>
>> I'm sort of used to a notation where
>>
>> G' is the new/scaled/denormalized/fudged value of G
>>
>> which is what the filter folks do. But maybe that's not an accepted
>> convention.
>>
>>
>> John
>>
>
>Oh, so S is the number by which things are divided, the divisor, and has
>nothing to do with that Laplace stuff?
>
>DNA
>*

Well, I did specify that Somethingorother was the divider in the loop, so it was perfectly obvious to me that $S = \text{divider ratio}$. There's only 26 letters on my keyboard, and it's not my fault that some lunatic Frenchman decided to use S for something else.

Actually, I never use that Laplace stuff. I must have learned it once in ancient times, because I didn't flunk very many of my EE courses, but nowadays a quickie Bode plot is enough to stabilize simple loops, and if it gets more complicated, or gets nonlinear, I just simulate.

I had an engineer a while back who was a whiz at this stuff... pages of equations, root locus, polynomials in s-domain, all neatly solved. But the answers usually made no sense, and when I pointed it out to him he got pissed off (ie, angry in American.) As soon as I finished paying for the legal fees to get him a green card, he quit.

John