

Re: PWM Amp Design

Source: <http://sci.tech--archive.net/Archive/sci.electronics.design/2005-04/msg02044.html>

- *From:* "Larry Brasfield" <donotspam_larry_brasfield@xxxxxxxxxxxx>
 - *Date:* Mon, 11 Apr 2005 07:43:11 -0700
-

"Genome" <ilike_spam@xxxxxxxxxxxx> wrote in message
[news:V1t6e.6093\\$C2.5422@xxxxxxxxxxxxxxxxxxxxxxxxxxxx](mailto:news:V1t6e.6093$C2.5422@xxxxxxxxxxxxxxxxxxxxxxxxxxxx)

>
> "Larry Brasfield" <donotspam_larry_brasfield@xxxxxxxxxxxx> wrote in message
> [news:Gcd6e.12\\$F24.425@xxxxxxxxxxxxxxxxxxxxxxxxxxxx](mailto:news:Gcd6e.12$F24.425@xxxxxxxxxxxxxxxxxxxxxxxxxxxx)

>
> [Garbage Spice Simulation Snipped]

>
>> The above simulation should be a convincing demonstration
>> that using the controller to get the PWM filtered output
>> response apparently desired by the OP is feasible and
>> unlikely to present serious problems. Obviously, gains
>> and maybe offsets will need adjustment once the VCVS
>> is replaced by the PWM IC. When current limiting is put
>> into place, some attention to limiting in the controller will
>> be in order. A sensitivity analysis for L and C variation
>> would be smart. It might be a good idea to make sure
>> no limit cycles are possible, using time domain simulation
>> and a range of step inputs.

....
> Let's just see the error report for your circuit,
>
> Questionable use of curly braces in "c1 vx 0 {7.2?/lpfs}"
> error: Error: unknown token in: "7.2[?]/lpfs"
> Questionable use of curly braces in "l2 va vx {22.5?/lpfs}"
> error: Error: unknown token in: "22.5[?]/lpfs"
> Questionable use of curly braces in "b1 va 0 v={{gx}*v(vc)}"
> error: Error: undefined symbol in: "(gx)*[v](vc)"
> Circuit: * C:\news\carlen\larry.asc
>
> Error on line 4 : c1 vx 0 (7.2?/lpfs)
> Unknown parameter "/lpfs"
> Error on line 5 : l2 va vx (22.5?/lpfs)
> Unknown parameter "/lpfs"
>
> Spice doesn't generate these sort of reports for general entertainment. It
> gives you indications about ERRORS in your circuit.

My simulation ran without diagnostics. There were

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no '?' characters in the file I pasted into my post. After filtering your post for useful content, I can see that some process between my clipboard and the post retrieved into my newsreader has replaced certain ASCII characters with '?'. That is something worth knowing, so, despite your caterwauling post, I thank you for the tip.

- > The analysis might run
- > but there is the old adage about 'garbage in, garbage out'.

Such wisdom. Another gem.

- > Shall we try again?
- >
- > Instead of 7.2 μ /LPFS try 7u2/LPFS
- > Instead of 22.5 μ /LPFS try 22u5/LPFS
- > Instead of .param LPFS=.1 try .param LPFS=1
- > Instead of $V=\{GX*V(VC)\}$ try $V=GX*V(VC)$
- > L1, that 250 μ inductor will be interpreted as a 250H inductor. Try the
- > proper value of 250u.
- >
- > You could write $V=80*V(VC)$ for B1 and include a note to the effect that you
- > are assuming that the peak to peak amplitude of the modulator triangle wave
- > is 2V and you are assuming a bridge supply of 80V. Then you might as well
- > just use the proper values for the components.

I could, but that goes beyond the stated purpose of my post. I could design the whole circuit, but there would be no purpose to it beyond a silly attempt to impress you and your ilk.

["... stupid ..." questions cut.]

- > Oh, R2 serves no visible purpose.

It does if a behavioral voltage source is the only consumer of what drove R2.

- > So..... Let's just fix and tidy up your circuit.

[Cut circuit which also suffered from posting path issues, but does simulate with group delay performance way outside of anything the OP stated or implied.]

- > Much prettier.

So you say. To simulate the PWM, I would revert the VCVS back to a behavioral source so that the PWM delay characteristic could be added.

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- > You're doing it again, I've told you about this before. You are plotting the
- > closed loop response rather than measuring the loop response. See how I've
- > inserted an AC source, VAC, in the loop.

The loop gain is not especially interesting, being readily determined by inspection. I made no effort to plot it.

- > Do an AC analysis, the circuit as given is set up to do that, and plot
- > $V(\text{VERR})/V(\text{VC})$. Notice how it crosses over at 400KHz with little to no phase
- > margin.

What you call VERR is not what is commonly called the error. As for doing AC analysis, I don't know quite what you simulated, but my controller, with loop gain set to bring the complex poles well into the LHP, has plenty of phase margin and a well behaved step response.

[More of same cut.]

[More folderol cut.]

—

—Larry Brasfield

email: donotspam_larry_brasfield@xxxxxxxxxxxxx

Above views may belong only to me.

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• *References:*

- ◆ ***PWM Amp Design***
 - ◇ *From:* Chris Carlen
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 - ◇ *From:* Chris Carlen
- ◆ ***Re: PWM Amp Design***
 - ◇ *From:* Larry Brasfield
- ◆ ***Re: PWM Amp Design***
 - ◇ *From:* Larry Brasfield
- ◆ ***Re: PWM Amp Design***
 - ◇ *From:* Genome
- Prev by Date: ***Re: Colloidal silver generator?***
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