

# Re: Instruction And Data memory

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I assume you are looking at a processor that has support for such things (or a system that has such a processor or MMU).

The difference is that instruction memory is exactly that: memory referenced during an instruction fetch (the newer processors discriminate between the various bus cycle types) and data memory is for just that: data.

There are a number of reasons for this, and they have separate origins.

Access level control. In a processor that supports the notion of privilege levels (the vast majority of 32 bits devices and up), I-memory can be marked as read-only at user level (so a program may not modify its own code), and writeable only by supervisory level(s), usually an OS function – for instance, the OS has to write that memory to load the program in the first place.

Data memory, on the other hand, is expected to be modified by a program, so the access to it is freely given to its parent process (although other processes may not be given access – this subject has books written about it).

Cache efficiency. Most processors have a D-cache and an I-cache. A cache holds recent instructions and data (and I am not going to get into just how recent or what type of algorithm – there are tomes out there on that).

If a cache has to be refilled, it's primarily for one of two reasons (there can be others): either the data required is not in the cache (a D-cache issue) or a branch/jump just invalidated the cached instructions, requiring an I-cache refill. As these two things do not happen synchronously (they do happen at the same time occasionally, but they are not statistically synchronous), separating the two makes sense to optimise the cache system.

That's a very broad brush overview of a complex subject, leaving out a huge amount of background, but it should give you the flavour of the idea behind it.

Cheers

PeteS

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      - ◇ From: thejim
  
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