

Re: Q to Win re:oscillation in high-voltage MOSFETS

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-06/msg04182.html>

- *From:* Robert Baer <robertbaer@xxxxxxxxxxxxx>
 - *Date:* Wed, 29 Jun 2005 18:40:26 GMT
-

Winfield Hill wrote:

Robert Baer wrote...

I have tried the models for the FQD2N100TM FET and have some questions.

1) The $\log(I_s)$ vs V_{gs} relationship does not hold below about 1mA, and I need that to work to at least 1uA; preferably to 10nA.

2) I see nonlinear *gate current*: 10uA at 0V, 0uA at 50V with "knees" near 5V and 9V. I had the mistaken impression that gates were insulated from the channel, and that there were no batteries inside FETs.

3) Could you please provide a resistive SPICE single-FET circuit that might oscillate?

You're asking about the model I posted, the second one? That model is supposed to work correctly, even to the nA region. Actually, as I said, I developed my own modified MOSFET model before Steven Sandler's paper came out, so it's different from his style, which was what I posted. That is, I didn't run his model in my extensive tests, having completed my 2500V amplifier analysis before his paper. So I'll have to go back and test and evaluate his model to verify its proper operation, and to observe the problems you mention above. This will take more

Re: Q to Win re:oscillation in high-voltage MOSFETS

time than
I have right now, so I'll see if I can do it this coming
weekend. But
don't hold your breath, because now I'm getting into the
intense work
rampup prior to my going away on vacation. This may therefore
be a
subject visited far in the future. But you could email me the
circuits
you played with and I'll put everything in a folder to examine
later.

Actually, *both* suck.

Try a resistor from Vgs sweep to gate, another resistor from drain to
fixed Vdss.

Start with low values and play mostly with the gate resistor.

.