

Re: this is getting crazy

We have given up on autorouters. Even Spectra can't manage to do a decent job on our dense boards, and managing signal integrity after autorouting is a nightmare. So now we manually route boards, even with 1,000+ components. Believe it or not, it takes us less time and it costs us less in the long run.

Oh, I do believe it.

We have found that the key to a (relatively) painless layout is lots of planning prior to routing.

Placement, placement, placement.

I always select pinouts on CPLDs, FPGAs, resistor networks and connectors (where possible) to make the layout as easy as possible. It takes time to do this, but this time is saved during layout. This approach provides shorter signals with fewer crossovers, which is always a good thing.

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As I said, we let our layout guy do it. He does an excellent job, even though he doesn't understand the functionality at all. We review it along the way to make sure it will be electrically nice.

I try to select component packages that will provide for the best physical flow of signals on the board. In this respect a larger component package may provide better real estate utilization and/or signal flow than a smaller package. Thinking about all of this stuff during the schematic phase pays off huge dividends later.

Right.

The three most important things about real estate are location, location and location. This applies to circuit boards too. I group parts in OrCAD to make the initial placement easier. For critical groups we may even route and lock it prior to placing other components. We spend lots of time on the group and component placement. A well placed component is an easy to route component.

I group nets in OrCAD so that these can be easily seen during routing. Also, I prepare a list of critical nets (clocks, strobes, resets, diff pairs, etc.) so that these can be properly managed.

With this approach we save time on design, save layer count, and reduce the risk of having another board spin because of signal integrity problems.

The thing that doesn't work is the "throw it over the wall" method you see in big companies or with outside contractors. While a serious

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board is being laid out, we work with our layout guy constantly, and we discuss things, and we often change the design to help him make a beautiful layout. 16-bit bus too nasty? OK, we can live with 8.

John

Treasure your layout guy. He's a rare find IMO. I'm firmly in Gregs camp, I do the layouts myself (hey, I get paid by the hour :) because it ends up faster than trying to explain things to the layout guy. I've had some terrible experiences in the past :(

I also do a crosstalk analysis, pre- and post-layout. Then measure it on an un-populated PCB, just to be sure. Peer reviews (harder as there is only me) to catch all the deliberate mistakes - I have a long, long list of things to look for, perhaps 20-30 per component type, as well as a list of all fuckups I have ever made or been witness to, to ensure they dont sneak back in. That way, I get to spend all of my debug time working on new mistakes, rather than re-hashing past cock-ups. And when a design is finished, a lessons-learned review pops those mistakes into my peer-review checklist - eg I will never use another opamp without measuring its PSRR, having been bitten badly by a TL064, which had *gain* at the frequency of concern :(

One day when I'm rich and famous, I'll get to use gazillion pin BGAs. We recently did EMC compliance testing on a PCB with a 55W planar smps, micro & CPLD. lovely ground planes (no slots at all), back-terminated clock line (15mm long), etc. the smps was quiet, but the TQFP144 CPLD package spewed out bucketloads of noise - confirmed by shielding the package, which fixed it. not a very large die, nice long bond wires. Luckily its expensive and hard to get, too :)

Cheers

Terry

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