

I2C "SCL" line problem

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Hi all,

I faced the following problem with my I2C slave code(VHDL).

I was incrementing a counter on the negative edge of SCL(this clock is coming from the processor's I2C port , 100 KHz frequency).

But what i observed on the CRO was that my bit counter which was running on the "negative edge" of SCL , was incrementing on "positive edge" also and this was not happening always.

The solution to this problem was i inverted the incoming clock "SCL" and used the rising edge to increment my counter now it was fine.

Can any I2C experts clarify what is the problem with working on "negative edge of "SCL" clock.

Regards,
Prav

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