

Re: Please suggest a time delay toggle switch

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2005-09/msg01806.html>

- *From:* mingyan_chow@xxxxxxxxxxxxx
 - *Date:* 7 Sep 2005 20:26:36 -0700
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John, I'd very much appreciate your design. That is certainly a professional design. In your circuit diagram, U3 is a dual oscillators for 33 and 45. U1 is for power on reset status. U2 AB is the time dealy switch. U2 CD is a toggle switch. U4 ensure there is only one clock signal will be pass to output. Am I right? Excellent. This circuit is very useful for me.

Please forgive me raising some new issues. As I digging deeper, more questions is beuing raised. Both 33 and 45 ouput signals need to be adjusted to a certain level. Therefore, 33 and 45 clock signal has to be rectified and go through a variable pot .I found the original circuit has a output of 1V P to P rectified signal feed to the voltge follower. In this case, U4 gate may not be appropriate.

- *Follow-Ups:*

- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* John Fields

- *References:*

- ◆ ***Please suggest a time delay toggle switch***
◇ *From:* mingyan_chow
- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* ehsjr
- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* mingyan_chow
- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* Fred Bloggs
- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* mingyan_chow
- ◆ ***Re: Please suggest a time delay toggle switch***
◇ *From:* John Fields

- Prev by Date: ***Re: Bush is either a liar, or an idiot, or both.***
- Next by Date: ***Re: Isolated power supply design***
- Previous by thread: ***Re: Please suggest a time delay toggle switch***
- Next by thread: ***Re: Please suggest a time delay toggle switch***

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- Index(es):

- ◆ *Date*

- ◆ *Thread*