

Re: Input stage mess

```

||||| .-----|____|-.
10u | J1 |---| +---|J2 ||| R2 |
||||||| ____ | \ |
in ---||---+--->|---| +---|<-----+---|____|-. | .----|+ \ |
||||||| 5mA R1 | 5mA || | >---out
.- .- '---+---' || GND || GND .-|-/ |
||||| V V || | |
||||| .----- . ||
1M-'-'1G || Precision |---+---||---+
| | V | current mirror | .-
GND | 160mA '-----' ||
| to / ||
| 240mA /+|-GND'-'
'-----+---< ||
| \-|+---'
| \ |
'-||----'

```

J1 and J2 are 4 to 6 paralleled IF3602, no source degeneration (noise), running at 20mA/transistor.
R3 and R4 are one per transistor and 50R (1V across the Jfet, 1V across the R)

The feedback path has low impedance (1 fb path per jfet, 1R/27R).

As you can see, nothing terribly fancy. All lies in the details (like the subject of this post).

For the problem of interest here, it comes from the differential input voltage which rises 6dB/oct with a 90° shift wrt to the input voltage (due to the open loop gain pole) and the JFETs capacitances across the inputs (1.45nF between the preamp in+ and in-) which introduces another 90° shift for the current injected at J1 gate, hence the negative resistance. Exactly the same pb as an emitter follower loaded with a cap.

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Thanks,
Fred.

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- *Follow-Ups:*
 - ◆ **Re: Input stage mess**
 ◇ From: John Popelish
 - ◆ **Re: Input stage mess**

Re: Input stage mess

◇ *From:* John Larkin

◆ **Re: Input stage mess**

◇ *From:* Frank Miles

◆ **Re: Input stage mess**

◇ *From:* Phil Hobbs

• **References:**

◆ **Input stage mess**

◇ *From:* Fred Bartoli

◆ **Re: Input stage mess**

◇ *From:* John Larkin

- Prev by Date: **Re: How to freeze the balls off a brass monkey**
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