

# Re: Hans Camenzind's Book, Designing Analog Chips

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- *From:* Joerg <[notthisjoergsch@xxxxxxxxxxxxxxxxxxxxxxxxxxxx](mailto:notthisjoergsch@xxxxxxxxxxxxxxxxxxxxxxxxxxxx)>
  - *Date:* Thu, 16 Feb 2006 18:25:57 GMT
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Hello Jim,

Naaah. A MOSIS run is quite cheap. Each process has a "shuttle" run... multiple chip designs on a single wafer. Good cheap way for "proof of pudding".

The run isn't so expensive but there you have to do the full chip design from scratch. I know that this is your bread and butter but many times my clients shy away from that because of the design costs. If it were just one or two metal mask layouts it might be easier to convince them.

And I might add... he who complains about resistor values shouldn't be trying to design an I/C ;-)

Well, I am not complaining about tolerances since you can do ratios. It's ok if they are 30% or whatever but low power designs require at least one type in the 1M range. Dividers for low battery detect, other thresholds and so on. Can't do current sources everywhere, plus they eat from the rather small pool of NPN/PNP.

Regards, Joerg

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