

# Re: Digital Osci and Logic Analyzer

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- *From:* Rich Webb <[bbew.ar@xxxxxxxxxxxxxxxxxxxxxx](mailto:bbew.ar@xxxxxxxxxxxxxxxxxxxxxx)>
  - *Date:* Fri, 07 Apr 2006 15:51:04 GMT
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On Fri, 07 Apr 2006 15:08:34 GMT, [nico@xxxxxxxxxxxx](mailto:nico@xxxxxxxxxxxx) (Nico Coesel) wrote:

Rich Webb <[bbew.ar@xxxxxxxxxxxxxxxxxxxxxx](mailto:bbew.ar@xxxxxxxxxxxxxxxxxxxxxx)> wrote:

As a rule of thumb, estimate the useable bandwidth as being limited by one-tenth of the ADC sample rate, not one-half. That lets you recover (more or less) the fifth harmonic of the signal of interest right at Nyquist. For some commercial examples, there's the Fluke 199C: 2.5 Gsps, overall bandwidth 200 MHz; and Tek TDS2012: 1 Gsps and 100 MHz. So for your

I disagree here. Shannon says a signal can be reconstructed up to half the sampling frequency. The higher sampling rates of the examples you mention are probably used to use less bits for sampling and make the analog input filter easier to construct (an RC filter still won't do the job) to prevent frequency aliasing. Digital filtering does the rest.

Thought problem. Signal A is a 1 MHz sine wave, signal B is a 1 MHz square wave. Sample each at 2 Msps. Based only on the samples, and not on any a priori knowledge of the expected signal characteristics, what would the o'scope display at 1 usec/div'n?

Lets suppose I decide to buy a 1Gsps ADC(which isn't going to happen any time soon) and I have a probe that works properly with the ADC. How would I go about storing/streaming all those samples? This would require a memory chip be able to work down at 1ns or so? I was thinking I could use several gigs of pc memory in parallel to reduce the latency and increase total

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sample size to a few seconds... is this possible? What about encoding for a digital stream? do something like rle on the bit stream where 01 one would store 2 bits as one and its number of repetitions? (need to use 2 bits atleast so things like a clock signal are encoded efficiently)

You don't need to capture or store more samples than you need for one display screen.

Assume that your display area is 500 pixels x 500 pixels at ten divisions each for horizontal and vertical. No matter how fast you sample, you've only that area to work with. For each time step (vertical column) you have several choices.

I disagree again, the less memory you have the more difficult it will be to capture a problem. You'll need some pretty fancy triggering.

Ultimately, however many samples are collected at whatever resolution and at whatever rate, they're going to end up on a relatively low-res display (low-res at least as compared to an "infinite" resolution analog display). The 500x500 is just an example to make the numbers easy; most are probably based on 1/4 VGA, VGA, or XGA resolutions.

You can decimate your sample rate down to where you grab just one instantaneous sample at that tick and store/plot only that value. For example, at 1 msec/div and 50 pixels/div that's just 500 samples at a lazy 50 Ksps rate.

Which makes the oscilloscope totally useless to capture problems. A good DSO can store loads of samples which were sampled at the highest possible frequency.

True. I'm not saying that decimation is an optimal or even recommended approach, just trying to point out to the OP that in and of itself an ADC that's capable of high sample rates does not mean that it must always be sampled, stored, and processed at that rate, irrespective of the display resolution and rate.

It's not aimed at how DSOs from Tek or Agilent approach the problem but how a reasonable home-brewer might take a first step.

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