Re: Digital Osci and Logic Analyzer

Source: http://sci.tech−archive.net/Archive/sci.electronics.design/2006−04/msg00812.html

- *From*: Rene Tschaggelar <none@xxxxxxxx>
- *Date*: Fri, 07 Apr 2006 19:26:58 +0200

Nico Coesel wrote:

> Rich Webb <bbew.ar@xxxxxxxxxxxxxxxxxx> wrote:
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> > On Fri, 07 Apr 2006 15:08:34 GMT, nico@xxxxxxxxxxx (Nico Coesel) wrote:
> >
> > > Rich Webb <bbew.ar@xxxxxxxxxxxxxxxxxx> wrote:
> > >
> > > > You don't need to capture or store more samples than you need for one display screen.
> > > >
> > > > Assume that your display area is 500 pixels x 500 pixels at ten divisions each for horizontal and vertical. No matter how fast you sample, you've only that area to work with. For each time step (vertical column) you have several choices.
> > >
> > > I disagree again, the less memory you have the more difficult it will be to capture a problem. You'll need some pretty fancy triggering.
> >
> > Ultimately, however many samples are collected at whatever resolution and at whatever rate, they're going to end up on a relatively low−res display (low−res at least as compared to an "infinite" resolution analog display). The 500x500 is just an example to make the numbers easy; most are probably based on 1/4 VGA, VGA, or XGA resolutions.

> True, but it is very convenient to be able to scroll through a signal
> and zoom in/out without recapturing the signal.

Nico,
you should leave these guys some room for
improvement. Once the memory is there, it
is almoste done, the rest is software.
Provided the cpu has some code space free.

As additional improvement when there are 1k
samples per pixel, one can think of displaying
the mean, or the min, or the peak−peak at
each pixel. And a fourier tranform as second
shown trace.

Rene
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