

Re: Digital Osci and Logic Analyzer

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- *From:* "Abstract Dissonance" <Abstract.Dissonance@xxxxxxxxxxxxx>
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"Rich Webb" <bbew.ar@xxxxxxxxxxxxxxxxxxxxx> wrote in message
news:t5pc32hq62cmgjrqaq3ss4i7f4jdsvuq3u@xxxxxxxxxxxx

On Fri, 7 Apr 2006 02:43:39 -0500, "Abstract Dissonance"
<Abstract.Dissonance@xxxxxxxxxxxxx> wrote:

How complicated is it to create a simple pc based oscilloscope and logic analyzer(excluding the pc software)?

Does it just consist of getting a ADC and interface for sending the data to the pc? I'm looking at trying to make one in a similar way to what is done on this site:

<http://www.fpga4fun.com/digitalscope.html>

I figured that the main the parts are the ADC, the probe, and the method of sending the information(which I think is the hardest part at high data rates?)? I've seen some ADC's that have sample rates of over 100Mps which should give me a 50Mhz bandwidth? Although these aren't cheap I've also seen some upwards of 1Gsps that would give me a larger bandwidth if I needed it.

As a rule of thumb, estimate the useable bandwidth as being limited by one-tenth of the ADC sample rate, not one-half. That lets you recover (more or less) the fifth harmonic of the signal of interest right at Nyquist. For some commercial examples, there's the Fluke 199C: 2.5 Gsps, overall bandwidth 200 MHz; and Tek TDS2012: 1 Gsps and 100 MHz. So for your

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Hmm. The Shannon sampling theorem says you only need to sample 2x to reconstruct the sample exactly? (i.e., need to sample twice as fast as the bandwidth you want to capture?)

Lets suppose I decide to buy a 1Gbps ADC(which isn't going to happen any time soon) and I have a probe that works properly with the ADC. How would I go about storing/streaming all those samples? This would require a memory chip be able to work down at 1ns or so? I was thinking I could use several gigs of pc memory in parallel to reduce the latency and increase total sample size to a few seconds... is this possible? What about encoding for a digital stream? do something like rle on the bit stream where 01 one would store 2 bits as one and its number of repetitions? (need to use 2 bits atleast so things like a clock signal are encoded efficiently)

You don't need to capture or store more samples than you need for one display screen.

? not for a digital logic analyzer? Also It would be nice to have some memory even for an oscilloscope since one might want look at the history of the signal? Maybe even zoom in and zoom out would be nice?

Assume that your display area is 500 pixels x 500 pixels at ten divisions each for horizontal and vertical. No matter how fast you sample, you've only that area to work with. For each time step (vertical column) you have several choices.

You can decimate your sample rate down to where you grab just one instantaneous sample at that tick and store/plot only that value. For example, at 1 msec/div and 50 pixels/div that's just 500 samples at a lazy 50 Ksps rate.

You could take, say, ten equally spaced samples within the column interval and plot the mean or median value. For the 1 msec/div example, that's acquiring 5000 samples at a 500 Ksps rate.

Or, sample at full rated speed for the entire sample interval and plot the extremes. If that's handled at the front end, only two values per column need to be sent or stored

I'm kinda curious to how high speed logic analyzers overcome some of these problems?

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By only needing to store a 1 or 0 for each sample point, and often by not storing every sample, just the transition times.

but if you have 1Gsp/s as some ADC's run at then that's storing 1Gb/s... so for 10 seconds for digital logic capture for a logic analyzer you would need 10Gb/s or about 1.25GB/s... and that's just for one channel ;/

Another thing I wanted to know is how digital logic signals are "sampled" in logic analyzers? Surely one doesn't need anything more than a 1-bit ADC to convert the line signal? (therefor one doesn't even need an ADC since it would act more like a buffer than a real ADC?)

I was thinking about buying a ADC that does about 40Msp/s and try it out just to see if it was going to work but and make a homemade probe to play with it. It doesn't seem like a terribly complex project but there seems to be a lot of technical issues involved.

New gizmo that might be of interest (although at about 2 Msp/s)
<http://www.quickfiltertech.com/html/qf4a512-dk.php>

Mouser has the dev kits in stock. Related article at
<http://www.circuitcellar.com/library/print/0306/Cantrell-188/index.htm>

More targeted at data acquisition and analysis than as an o'scope core but would give you a working platform to experiment with.

Yeah... but I don't see it being really any different than what I have mentioned at the top... They do the post filtering on the device but that can easily be handled by the pc. I'm just interested in getting the data to the pc where I can then have as much fun with it as I want.

The sample rate bothers me though as it's too low for what I need. I want to sample at least a 40MHz signal so this won't help much and all it seems like to me is a glorified ADC.

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Rich Webb Norfolk, VA

Re: Digital Osci and Logic Analyzer

Thanks,
Jon