

Weekend one-shot timer design

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While idly contemplating oscillators, I thought I might want to try a controlled delay oscillator. That is to say, one thing runs this much time, then another, then another, then another, then back to the first. My thought was to have two long "ON" delays spaced with short delays for MOSFET switching/"OFF" time. One way to do this would be a chain of one-shot timers.

I like discrete, and I like short circuits. I figured, hmm, this is going to need a flip-flop, because it is a state machine after all, and I'll need a capacitor charger, discharger, and a comparator of some sort. The charge can come from a resistor or CCS, simple enough. The discharge could be turning off the CCS, and, uh, well hell let's just clamp CCS and cap together, that'll save a pair of resistors.

For comparator I could wire up a seven transistor op-amp, and more than double my parts count, but hell, there's gotta be an easier way. Ya know, isn't it nice that a transistor only conducts when the base is forward biased? Fair enough! Now I just need some way to make that work, hmm a zener on the emitter will set trigger voltage solidly, I could use a collector resistor to drive the next transistor but saturation is slow, especially for low drive currents, ah let's throw in two base diodes and an emitter resistor. Now it switches over 0.8V or so, much slower, but output current is far more consistent. Now I can drive a base directly.

Since this NPN is already a few volts above ground, and it doesn't work terribly fast in absolute terms, I'll toss on a PNP to drive the flip-flop. Ah, that crisps things up nicely.

<http://webpages.charter.net/dawill/Images/One-shot%20Timer.gif>

Overall, seven transistors. I could probably make it work with five, but I tried and the flip-flop was being very finicky about reverse bias from the trigger input (yeah, DTL would probably fix that). So I went with the pair of RTL NOR gates. And, I like RTL. :-p

Specs:

$C_t = 0$, $R_t = 1\text{mA CCS}$: pulse width $0.8\mu\text{s}$, maximum repetition rate 700kHz. Pulse width is maintained down to individual cycles, as near as I can tell, at least as long as the rising edge is fast enough to pass the 220pF (my sig

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gen has no shortage of speed for that).

$C_t = 1000\mu\text{F}$, $R_t = 60\mu\text{A CCS}$: pulse width approx. 80 seconds (suggesting capacitor is actually $1240\mu\text{F}$;-). Decision made in roughly 0.1s, and fully discharged in 0.1–0.2s. (It's fun to watch the voltage cross 4.20V, pause for a moment, then quickly scan down to zero. –If that voltage is odd, it's because I'm using a pair of red LEDs, since I don't have a 3.3V zener on hand.)

Because the circuit is edge-triggered, it ignores cycles during charging. Thus, the circuit is useless as a missing pulse detector. However, this has an interesting consequence, as the dead time inbetween output pulses directly corresponds to the input frequency, since for rates higher than the timing rate, one or more cycles are skipped. I'll have to watch this some more to figure out what the implications are, but I would suppose harmonic frequency division or something would be the idea. In this manner, with $C_t = 0$ and $R_t = 1\text{mA}$, the maximum input frequency is around 2MHz, above which the output rolls off because the drunken input 2N4401 slurs the pulses together.)

Haven't yet built another (geez, I'm out of 1k resistors!), but two together, linked by the Q' output, should be a straightforward multivibrator (though with the cap and diode input network, it will need a starting pulse), and three or more should make a polyphasic squarewave output. Multiple modes may even be possible, as varying numbers of pulses cascade through what is effectively a looping shift register. Oooh, a megabyte of these would make a skookum digital delay line...

Tim

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Deep Fryer: a very philosophical monk.

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