

Re: SMPS, control loop?

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- *From:* Terry Given <my_name@xxxxxxx>
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Joerg wrote:

Hello Tim,

Well, say you have a load on the output, the system is in equilibrium, and you suddenly decrease the load. If the controller responds slowly (as it must in voltage mode), then the duty cycle will remain constant, pumping more charge into the filter inductor, also ramping up transformer current as well. Eventually, the filter capacitor will respond, but only after roughly an LC time constant, perhaps a millisecond or so (say, 50 cycles of the PWM frequency), at which time the inductor will theoretically have a metric shitload of amps through it! This energy then flows into the capacitor, so voltage keeps rising, a lot, and the controller chokes off the PWM until capacitor voltage falls to a reasonable level, at which point the voltage continues to drop, because it then takes more time to recharge the inductor.

Thou shalt not provide too small of a load side capacitor. So don't play uncle Scrooge with that cap ;-)

If the controller is current-mode, duty cycle can be controlled directly by current and somehow secondarily by voltage, but voltage will still overshoot as the inductor's excess energy plops into the capacitor.

In some constellations (small cap, >50% duty) this can result in stability issues. You can read up on that under the topic "right half plane zero" or "RHP".

But neither the KA7500 or SG3524 (both used in AT supplies) are naturally current mode. I don't see obvious evidence of a current shunt and amplifier to convert output current to error voltage, though I haven't thoroughly traced the

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schematic.

Current mode control prevents the inductor current to reach "kablouie" levels. I usually employ current mode in my (often discrete) designs.

Regards, Joerg

As usual, Joerg is spot on. Jerald Foults' website (spelling?) has a whole bunch more useful stuff. (P)CMC is the way to go. If only the UC384x was developed before the poxy SG3524 or TL494....

NB: real men dont use smps chips ;)

As long as the peak energy stored in the output cap(s) is \gg that in the choke, the overshoot is small. If electrolytic caps are used and ESR is minimised, capacitance tends to be very high (multiple larg