

Re: AD7714 help

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- *From:* "Prakruthi" <prakruthi.rao@xxxxxxxxxx>
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Arlet wrote:

Prakruthi wrote:

I did compare the signals with the clock and found out that the data is not getting transferred on the right clock edge. How do I set the clock sync right. How do I determine what the right clock frequency for the SPI transfer would be.

I m using the ATmega8 to communicate with the AD7714. So it has amazing options for configuring the SPI clock frequency. The ATmega8 runs at a frequency of 14.567MHz. And im using a SCLK frequency of felkin/128 to drive the slave(AD7714), with a CPOL=1 and CHPA=1. I have no idea what the problem could be , cause I have tried all the different SCLK frequencies that are available.

The clock frequency is within limits, and CPOL=1, CHPA=1 is also correct.

What makes you say the 'data is not getting transferred on the right clock edge' ?

I can see constant clock signals on the oscilloscope for SCLK and DIN and DOUT shows data transfers, but the DRDY acknowledge pin on the AD7714 sometimes just shows noise and sometimes shows a low(which is an indication of dataword being available at the output register of the AD7714) after several several clock cycles.Do you understand what I mean?