

Re: PID question

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- *From:* hondgm@xxxxxxxx
 - *Date:* 22 Nov 2006 15:08:02 -0800
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John Popelish wrote:

hondgm@xxxxxxxx wrote:

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hondgm@xxxxxxxx wrote:

digitally regulating voltage.

Understood. In PID controller terminology, the DAC produces a setpoint for the voltage regulator. The regulator acts as a follower to copy the reference as the voltage output (possibly with a scaling factor).

I'll be able to set the voltage via a user interface (as well as current), but the PID controller will have the capability of forcing the voltage lower to meet a current setpoint.

a lot like preventing integral wind up in the master control of a cascade control strategy (the voltage control, in this case) when it loses control of the slave (the current controller). In effect, you need some way to limit the error at the input of the error amplifier, once the output ceases to have an effect (the moment the current limit process takes over), so that voltage control resumes smoothly and quickly, once the current falls below the limit value. Limiting the integral windup causes the voltage controller output to match the current limit setpoint at the moment that the current falls below the current limit value.

Re: PID question

Yes, integrator windup, I just read about that after I wrote the email. That part I now understand. But I'm unclear about a couple things in the topology. Here's a drawing of how I understand it:

<http://www.yourfilehost.com/media.php?cat=image&file=Drawing1.jpg>

I wasn't sure about where the feedback goes. One problem, if the feedback path is correct as I have it, is that my current range is 0–2500 and the current range is 0–4000. Maybe it just has to be scaled.