

Re: PID question

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On a sunny day (Thu, 23 Nov 2006 11:17:16 -0500) it happened John Popelish <jpopelish@xxxxxxxx> wrote in <uNSdndvqFuG6WvjYnZ2dnUVZ_h-dnZ2d@xxxxxxxxxxxxxx>:

hondgm@xxxxxxxx wrote:
(snip)

On your next post where you say that "you must allocate several samples to your desired response time", do you mean that I should be taking an average of several samples before feeding it into the PID loop?

(snip)

Not at all what I think he meant.

Each sample you take must be used as quickly as possible, to minimize time delay inside your control loop.

I think what he meant was that it takes many cycles of your sample and control algorithm to restore the system to setpoint, after a disturbance, so just because you can sample and cycle your program 100k times per second, don't expect to recover, completely, from a step current error much faster than 10 to 100 sample times (100us to 1000 us), especially with load impedances other than for what the control loop tuning was optimized.

Question:

I am a bit confused here, this comes from my experiments with fast digital PLL locking, say all is normal, no current limit active.

Then he connects some load (let's say R only) and the sampled current point at t_0 reads 1A.

Because it is digital he KNOWS (from the DAC) the voltage. Say the voltage was 10V.

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He now can calculate he has a 10 Ohm impedance, and this calculation is available at t_1 (few micro seconds later).

If the current limit setpoint was 100mA, he then sets the DAC at t_2 to an output voltage of 1V.

The next sample read at t_3 will be 100mA and balance will have occurred.

With inductive or capacitive load you will get no balance that quick of course.

But the basic calculation should converge fast (An ideal L on output would lead to 0V (divide by zero error ;-), an ideal C on output would lead to 100% V_{out}).

This is not exactly PID is it?

Is this correct?