Re: PID question

Source: http://sci.tech−archive.net/Archive/sci.electronics.design/2006−11/msg04851.html

- *From*: John Popelish <jpopelish@xxxxxxxx>
- *Date*: Thu, 23 Nov 2006 13:30:20 −0500

Jan Panteltje wrote:

> On a sunny day (Thu, 23 Nov 2006 11:17:16 −0500) it happened John Popelish
> <jpopelish@xxxxxxxx> wrote in
> <uNSdndvqFuG6WvjYnZ2dnUVZ_h−dnZ2d@xxxxxxxxxxxx>:
>
> > hondgm@xxxxxxxxx wrote:
> > (snip)
> >
> > > On your
> > > next post where you say that "you must allocate several
> > > samples to your
> > > desired response time", do you mean that I should be taking
> > > an average
> > > of several samples before feeding it into the PID loop?
> >
> > (snip)
> >
> > Not at all what I think he meant.
> >
> > Each sample you take must be used as quickly as possible, to minimize time
> > delay inside your control loop.
> >
> > I think what he meant was that it takes many cycles of your sample and
> > control algorithm to restore the system to setpoint, after a disturbance, so just
> > because you can sample and cycle your program 100k times per second, don't
> > expect to recover, completely, from a step current error much faster than 10
> > to 100 sample times (100us to 1000 us), especially with load impedances
> > other than for what the control loop tuning was optimized.
>
> Question:
> I am a bit confused here, this comes from my experiments with
> fast digital PLL locking, say all is normal, no current limit
> active.
> Then he connects some load (let's say R only) and the sampled

current point at t0 reads 1A.
Because it is digital he KNOWS (from the DAC) the voltage.
Say the voltage was 10V.
He now can calculate he has a 10 Ohm impedance, and this calculation is available at t1 (few micro seconds later).

If the