

Re: 20–60A adjustable ~200vdc current mode buck design

Source: <http://sci.tech–archive.net/Archive/sci.electronics.design/2007–02/msg03987.html>

- *From:* "John Barrett" <ke5crp1@xxxxxxxxxxxx>
 - *Date:* Wed, 21 Feb 2007 02:07:59 GMT
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"Genome" <mrsspamizgood@xxxxxxxxxxxx> wrote in message
[news:JiNCh.8926\\$fa.8795@xxxxxxxxxxxxxxxxxxxxxxxxxxxx](mailto:news:JiNCh.8926$fa.8795@xxxxxxxxxxxxxxxxxxxxxxxxxxxx)
<<SNIP>>

Oh..... OK, fiddle fiddle fiddle. Try one of these,

<http://www.genomerics.org/laser/pfcpar.asc>

That's two stages operated in parallel with the clock waveforms shifted. The idea is sort of that the current error amplifiers receive the same demand signal from a single or master voltage error amplifier and program the same current in their respective power stages. You have to figure out how to tie the available parts in the ICs together to do the job.

One thing you are forced to do is use current transformers to recreate the inductor current. At high powers this would be done anyway but at low powers you would use a sense resistor in the return lead to the input rectifier. Unfortunately when you try to operate things in parallel you can't do that any more.... they just won't connect together proper like.

I've added some source sense resistors to the 'mosfets' but not implemented a current limit with them. Problem is that the drain current transformer is operated at high duty cycles and might saturate. You lose the signal and things go bang. Resistors don't, lose signals, so it's a kind of 'oh shit!' protection.

The peak limit is simplified a bit. It really needs slope compensation but the IC does not make that easy to add, that's why those transistors were in the previous one. Here I've just thrown in some appropriate current sources.

I've diddled it to do 1KW per section from a 220V line..... I suppose you will need 8 of them because you are some sort of cross dressing freak. There are ways of synchronising these ICs by shoving a pulse up their oscillator. I'm sure if you read some data sheets you'll get some ideas.

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In the old days a 4017 Johnson Counter clocked at N (stages) times the desired base frequency with the reset pin on the appropriate tap did the job. These day I suppose you would use a PIC.

Really all you are getting is something to practice your sums on. You will probably find some of the values I've left in there are sub-optimal. You can try putting in 'real' components to get some guesses about power losses. I'd recommend you grab hold of some SiC diodes for the main boost diodes.

Have Fun and try not to go too fruit pie.

DNA

I've already located inexpensive isolated current sensors with models for 50 or 100 amps and 3000v isolation, so I can easily do high side current sensing — just gotta do a spice model for it, which looking at your models has helped me figure out (a voltage source defined via a formula referencing the load current)

I'm seriously looking at the PFC chip you mentioned, and some others (I've already tried to model out one using the LT1248 but its not working right yet)

You want fruit pie ?? here is fruit pie — what would it take if I wanted a true earth ground on the output of this mess — I've considered running seperate boosts on the poitive and negative outputs from the bridge, using the isolated current sensor to get EVERYTHING out of the ground path.. one of them inverting to get a positive voltage (add more in pairs if 2 wont get me enough current at reasonable ripple)

is that fruit pie enough for you ?? or is there a better way ??

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