

The Education of MassiveProng (Pt 3 of 275) (001/634) (588/634)

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speed of bus 104.

The PPU has a section 912 that incorporates the functionality of an 82206 peripheral controller chip. Included are two 82C37-compatible DMA controllers 910, two 82C59-compatible interrupt controllers 914, one 82C54 compatible timer/counter 916, and an MC146818-compatible real-time clock 918 with 114 bytes of CMOS RAM memory. A high-page register is included in the DMA subsystem to support DMA to a 32-bit memory address. The PPU provides an XD bus and control signals that are used to support BIOS ROM (including flash EEPROM) and keyboard

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