

Re: Timing in Synch Comm.

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- *From:* Vladimir Vassilevsky <antispam_bogus@xxxxxxxxxxxx>
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Jon Slaughter wrote:

How critical is keeping the timing relatively stable in synchronous communications?
Obviously the slave is synched to the master's clock but is there ever any problems if the clock timing is extremely unstable? Say varying up to 10% on average but even peaking to 100% or more in rare circumstances.

I'm writing a windows app which sends data to the parallel port but because its pre-emptive there can be extreme latency in the timing. The data is always synched with the clock so there is no issue with that but just of the clock's frequency varying a great deal. I imagine since its synchronous comm. that it should matter but just wondering if there are instances it could?

Lets say, for example, that its a clock at 1Mhz but then stops completely for several ms. Could this cause any problem with any device?

Yes, it can cause problems in some cases.

AVR Mega644 is indeed sensitive to the SPI clock irregularities while being programmed. It causes the programming to fail. I suppose the other new AVRs are sensitive to this, too. The older AVRs don't have this problem; you can interrupt the process at any moment for any long time.

I know its the nature of synchronous devices only to send/recv data on a clock transition and it would seem that frequency variations wouldn't matter but I just want to be sure that its not going to be an issue.

This can be the issue – it is a fact. We can only speculate why it happens; perhaps, the internal state machines may have a timeout protection or something. I didn't believe it before I encountered that problem myself.

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