

Re: Confused about synchronous communications

Source: <http://sci.tech--archive.net/Archive/sci.electronics.design/2007-09/msg03934.html>

- *From:* Jan Panteltje <pNaonStpealmtje@xxxxxxxxxx>
 - *Date:* Thu, 20 Sep 2007 22:43:15 GMT
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On a sunny day (Thu, 20 Sep 2007 22:33:53 GMT) it happened "Jon Slaughter" <Jon_Slaughter@xxxxxxxxxxxxx> wrote in <[lzCli.8208\\$JD.7462@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx](mailto:lzCli.8208$JD.7462@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx)>:

I guess what I'm asking is if the data needs only to be valid on the rising edge(or falling edge) of the clock and maybe a little after... and hence by having the clock rate 2x faster it will "sample" it in the middle of the data which means I have about 1/2 the clock to get the data there?

Imagine a 74HC74 D flipflop.

It is positive edge triggered.

If you put data on the D input, and send the clock from 0 to 1, that data will appear on the Q output.

After it has changed state (respect hold time) you can do with data what you want, and lower clock whenever you want (after min clock hold time).

Again look at the datasheets, it should be there.

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