

Re: Which university produces good analog EEs?

Re: Which university produces good analog EEs?

Source: <http://sci.tech--archive.net/Archive/sci.electronics.design/2007-10/msg01279.html>

- *From:* Joerg <notthisjoergsch@xxxxxxxxxxxxxxxxxxxxxxxx>
 - *Date:* Mon, 08 Oct 2007 15:11:39 GMT
-

krw wrote:

In article <a2ucg35u48ig1q4kj8s061tki8cnihu41t@xxxxxxx>, jjlarkin@xx says...

On Thu, 4 Oct 2007 20:36:08 -0400, krw <krw@xxxxxxxxxxx> wrote:

In article <[1c9Ni.5861\\$6p6.4832@xx](mailto:1c9Ni.5861$6p6.4832@xx)>, notthisjoergsch@xxxxxxxxxxxxxxxxxxxxxxxx says...

miso@xxxxxxxxxxx wrote:

[...]

Oh
yeah,
the
lack
of
soldering
skills.
That
would
require
the
student
to
have
actually
built
something.

Re: Which university produces good analog EEs?

These
younguns
just
know
how
to
program.
You've
seen
the
posts
where
a
pic
uP
is
the
solutions
to
any
task,
not
a
state
machine
comprised
of
memory
elements
and
combinational
logic.

For the vast
majority of
applications,
a uC is the
right
solution,
certainly
over the
discrete
implementation
you suggest.

I certainly would not say "vast". Many times
I have pondered the use of a uC in a design
only to come to the conclusion that 50c is

Re: Which university produces good analog EEs?

still too expensive. It's amazing how cheap
"poor-man's logic" can be.

You must have very small problems. I've never had one of those. ;-) The project I'm working on now is in a pair of XC2V-6000s (my part) and a couple of huge (don't know the model) Virtex-4s. I think I'm only going to fill 5% of it (and fewer I/Os), but...

What's the most expensive FPGA you buy?

The most expensive I personally spec'ed was an SCX600E in, IIRC '99, while they the Virtex-E family were still engineering prototypes. They were \$1200ea. As expensive as those things were, I had far more invested in software to program them than the chips themselves. Performance was an issue on that project.

I'm pretty sure the things I'm working on now are quite a bit more than that; 10x the size, twice the pins, and rated for UncleS.

Seriously, I think you're only looking at a small niche. I do believe uCs are the right solution for the vast majority.
...even the birthday card I got has one in it. :-/

It's fun, now and then, to design for flat-out performance, and damn the cost.

Often I've had projects where performance wasn't even the real issue. Like I said, cost rarely, if ever, was.

The problem with using a uP in such projects is if you are designing a chip, you need to know how to do it with gates as often that is the smallest and lowest power solution. The ability to hand craft logic is disappearing rapidly, but is very much needed in mixed

Re: Which university produces good analog EEs?

mode chips
which are not done on fine
geometry processes.

It sure is disappearing, just like analog skills
seem to be almost gone in fresh grad.

I've ripped out many uC solutions for
reliability and cost reasons. Same for
PALs/GALs because that's the era back in
the late 80's when mixed/discrete design
skills began to tank. The topper was a
system where I ripped out so many (plus
went to 100% AC terminations) that the
power supply kept tripping off and one of
them blew. We had managed to get
underneath the minimum load. IIRC the
PALs was guzzling 30–40mA just sitting
there. Each.

What's the old saying? If they only learn
how to use a hammer every problem will
begin to look like a nail. Heck, I've seen
one–shots being done with a uC. That
almost made me sick.

One shots make me sick too. ;-)/2

What? Another case of asynchrophobia?

More acousticophobia, but I'm not a NASCAR fan either. They go off in weeds. I don't like it
when my designs do. It usually causes long weeks (though I've been pulling 60hr weeks for a
month or so).

Brace yourself for 70 hours or more if the universities don't start cranking out engineers with more useful
hardware knowledge.

—

Regards, Joerg

<http://www.analogconsultants.com>

.

Re: Which university produces good analog EEs?