

Re: RC Transmission Lines (Wafer-Scale)

Source: <http://sci.tech-archive.net/Archive/sci.electronics.design/2007-10/msg03889.html>

- *From:* Guy Macon <<http://www.guymacon.com/>>
 - *Date:* Sat, 20 Oct 2007 16:40:17 +0000
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Guy Macon <<http://www.guymacon.com/>> wrote:

I have been doing a web searches on this, and found these:

The Future of Wires

<http://www.cs.utah.edu/classes/cs6943/papers/horowitz99future.pdf>

The Wire

<http://www.vlsi.uwaterloo.ca/~manis/ece730/lecture2.pdf>

Parasitic Extraction and Performance Estimation from Physical Structure

<http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/ch04/ch04.html#4.2>

<http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/toc.html>

I also found this in an abstract (the actual paper isn't online):

A 3Gb/s/wire Global On-Chip Bus with Near Velocity-of-Light Latency

"We successfully show the practical feasibility of a purely electrical global on-chip communication link with near velocity-of-light delay. The implemented high-speed link comprises a 5mm long, fully shielded, repeaterless, on-chip global bus reaching 3Gb/s/wire in a standard 0.18 μ m CMOS process. Transmission-line-style interconnects are achieved by routing signal wires in the thicker top metal M6 layer and utilizing a metal M4 ground return plane to realize near velocity-of-light data transmission. The nominal wire delay is measured to 52.8ps corresponding to 32% of the velocity of light in vacuum.

<http://www.google.com/search?hl=en&q=%22A+3Gb+s+wire+Global+On-Chip+Bus+with+Near+Velocity+of+Light>

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