

# Re: Debouncing....at About 1Mhz

*Source:* <http://sci.tech--archive.net/Archive/sci.electronics.design/2007-11/msg00062.html>

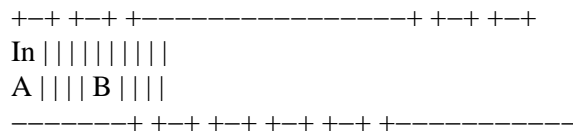
- *From:* John Fields <jfields@xxxxxxxxxxxxxxxxxxxxxxxx>
- *Date:* Thu, 01 Nov 2007 13:17:55 -0500

On Thu, 01 Nov 2007 08:17:25 -0700, John Larkin  
<jjlarkin@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx> wrote:

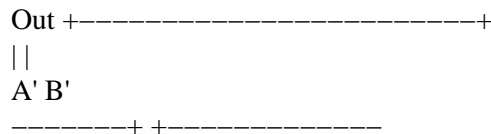
On Wed, 31 Oct 2007 21:53:15 -0800, D from BC  
<myrealaddress@xxxxxxxx> wrote:

This has got to be a classic signal clean up problem....

I need a circuit that triggers on edge A, then ignores about 0.1uS of jitter then triggers on edge B and then ignores a following 0.1uS of jitter.



|<0.1uS>| |<0.1uS >|  
|< 0.5uS >|



Edge A to A' is ~ less than 10nS  
Edge B to B' is ~ less than 10nS

All values are approximates.  
"In" and "Out" are repeating waveforms.

I think I can do it with:

- 1 flip flop
- 1 >0.1us delay circuit

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Sprinkled with gates..

Or maybe I need 2 flip flops..one for edge A and one for edge B..

I'm not even sure yet which type of FF to get.

If anybody has done this problem before and doesn't mind sharing..let me know a topology...

In the meantime, I'll be doodling until I get a solution...

D from BC

Looks like you can do it with a dflop, a quad xor, and an RC.

Run the input through a delay-line edge detector (three gates of delay, then xor) and clock the dflop. Then rc lowpass the input and apply it to D. Q is the output.

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Edge B to B' is ~ less than 10nS

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JF

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