

Re: Debouncing....at About 1Mhz

Source: <http://sci.tech--archive.net/Archive/sci.electronics.design/2007-11/msg01337.html>

- *From:* John Larkin <jlarkin@xx>
 - *Date:* Sat, 10 Nov 2007 07:46:46 -0800
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On Sat, 10 Nov 2007 09:13:06 -0600, John Fields
<jfields@xxxxxxxxxxxxxxxxxxxxxxxx> wrote:

On Fri, 09 Nov 2007 17:38:26 -0800, John Larkin
<jlarkin@xx> wrote:

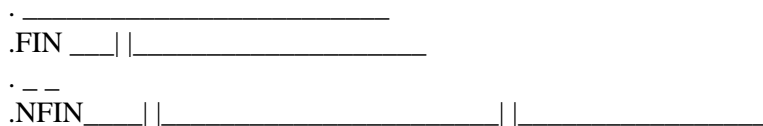
On Fri, 09 Nov 2007 18:46:37 -0600, John Fields
<jfields@xxxxxxxxxxxxxxxxxxxxxxxx> wrote:

Hazard free? There still remains the RFI issue from all that
chatter, which you haven't adequately addressed.

I was referring to timing hazards, which all of the hairball circuits
have. And I can't understand your fears about running signals through
gates. How are you ever going to do logic if you're afraid to run
signals through gates? "All that chatter" is in fact the input signal.

I'm surprised that you don't seem to know this, but if you have a
signal with sharp edges then, at each transition, a multiplicity of
harmonics will be generated and radiated into space.

Look at it like this:



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where FIN is the input signal and NFIN represents the spectral products generated by FIN's transitions, i.e. noise, if you have no use for the harmonics.

Now, if that signal is delayed by sending it through a gate:

```
|\
FIN>---| >--->DFIN
|/
```

we'll have:

```
. _____
.FIN ___| |_____
. --
.NFIN ___| |_____ | |_____
```

on the input to the gate, and:

```
. _____
.DFIN _____| |_____
. --
.NDFIN _____| |_____ | |_____
```

on the output of the gate.

Notice that there are now twice as many noise pulses as there were before, since there's one on each of the incident as well as the delayed transitions.

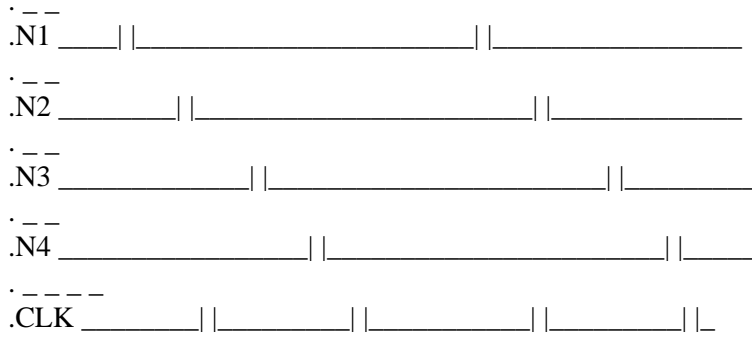
The chain in your circuit: (View in Courier)

```
N1
/
+-----A
| N2 Y---CLK
FIN>--+A / +--B
Y---A /N3 |
B Y---A |
| B B--+
|| Y \
|| | N4
GND>----+-----+-----+
```

(assuming equal gate delays) generates noise pulses that look, roughly, something like this:

```
. _____
.FIN ___| |_____
```

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with the result that your circuit (assuming edge rates equal to those of the comparator) is generating five times as much noise as the output of the comparator, FIN.

Do you know how much logic is on your PCs motherboard? Or in your keyboard, or your mouse? Do you think the designers avoided adding 4 gates because they would make "hash"?

When you design logic, do you actually avoid running signals through gates because gates cause emi?

I offered a circuit that has two cans and does everything the OP specified, and is timing-hazard free. And you're complaining that I'm using a quad xor gate to process his signal, and that's bad because it's an emi hazard. Preposterous.

John

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