

Re: Knowledge in DUP-line protocol?

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- *From:* JosephKK <joseph_barrett@xxxxxxxxxxxxxx>
 - *Date:* Fri, 23 Nov 2007 16:51:50 GMT
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Run.PDP nnc@xxxxxxxxxxxxxx posted to sci.electronics.design:

JosephKK wrote:

Run.PDP nnc@xxxxxxxxxxxxxx posted to sci.electronics.design:

<SNIP>

I do not
understand
your
difficulty.
Any device
on the bus
can change
any 0 to a 1.
All devices
on the bus
compare
what is on
the
bus to when
they are
trying to
transmit,
and will
thus know.

xmitr 1

xmitr 2

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bus

Thus xmtr 1
can see that
it is being
interfered
with. Now
where are
these
request bits
placed in
the
transmitted
block?

This is true for a generic
"Wired or" bus structure.

DUP-line is much more than
just two pull-upped wires
and some
transistors.

Amongst other things, there
is a "Bus-master" (so called
master-generator or
channel-generator) that is
continuously
controlling the bus by
sending frames, each
consisting of a
start-block and N bits of
information. By default,
these bits
are 0, but any device can
influence on the
channel-generator
for any bit, so that the
transmission of a 0 is
changed "on
the fly" to a transmission of

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a 1.

My questions are addressed
to anybody that has the
explicit
knowledge in this bus
technology, its timing spec
etc.

Best regards /Göran

Then why didn't you read what i posted. I
posted how to do part
of
the solution that you said you were missing.
I also directed
you to where to look for for the rest of the
solution.

Sorry for not explicitly pointing to the problem of your
answer.

The logic diagram you have attached is not correct. The bus
is
strictly wired-Or, active low. (Open collector). Thus, The
periods you have indicated late in the diagram, where T1
would
like to send High (the timing pulse part for the first 30% of
each bit-time), while T2 keeps low would on a real bus give
low
signal, ie the correct clock-pulse on the line is taken out by
the misbehaving T2 transmitter. (This should be obvious by
my
former writing). The T2 transmitter, if it wants to make one
pulse active will have NOT to interfere with the timing of the
master generator (for the next bit). – There is a window
within
one bit-time when a transmitter is allowed to pull low.

The question I still would like to have knowledgeable
answers to
is regarding the timing in this interaction between
"Transmitter
1" (master) and transmitter 2 (ie when may a transmitter start
pulling low, when must it start pulling low (first allowed and
last allowed time), and when may it release and when must it

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release...

I have described this in detail in my earlier texts.

I can also figure out how to experiment with one device, but that will still not answer to the design specifications. My hope was that some- one out there would happen to have read the true spec's some time!

Best regards /Göran

All the information is there. If you cannot see it perhaps the task is too difficult for you. It has to start pulling low by 0.3 clocks and hold it until 0.7 clocks, as per your description. Clock recovery by delay locked loop (edge sensing). Program or circuitry as required. Finding the right bit, byte, and frame are referred back to the student.

Thanks for this fine answer, that is of no use to me. As you have not revealed any previous knowledge in the protocol but just seems to be adding my questions together, I can't see any contribution besides your insolence.

You claims the sender has to start pulling low by 0.3 clock, I'd say it is allowable to pull down from 0.0 clock up until x, where $0.x < x < 0.7$ clocktimes. A requirement of action at an exact point in time would be most unstable for a distributed system.

You claims the sender will have to keep low until 0,7 clocks, I'd say the opposite, as the channel/master-generator will perform the task of prolonging the pull-down time to the right timing and length, once it has realized someone on the bus wants the actual bit to be set (ie low).

No, the bus master is responsible maintaining the low going edge. And all devices for sensing the bus at 0.5 +/- 0.05 clocks. (Got to stay away from the edges)

That way, a sender will get acknowledge of proper transmission within the same bit that it initiates - which would be truly impossible with the scheme you suggest.

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It gets verification by monitoring the bus while it transmits.

And at the same time, the bus is more robust, as timing is performed at one point, not at every connected sender.

My guesswork is that the sender should be pulling low like 0.15 to 0.45 clocktime, both ± 0.1 clocktime in order to safely have the bus pulled at 0.3, and to be safe of not disturbing the important timing performed by the master. An ack. of fulfilled active transmission can be seen by checking the state of the bus at 0.6 ± 0.05 clock. Please note that this is an assumption, that has not been confirmed by proper knowledge.

If you are admitting your assumptions but not the logical consequences thereof.

One has to realize that esp. the distributed devices might be timed using a simple capacitor timer, and they might be placed in "outdoor temperature", thus timing is everything but constant. Despite this, the bus has been around for like 20 years, and it has a reputation of being indeed very stable. This can only be achieved with a protocol that is robust and forgiving!

Regards /Göran

I offered to help you see the circuitry for what you described, but you are not listening.

Maybe you can post a link to the protocol definition.

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