

Re: Gate drive resistor question.

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- *From:* Terry Given <[my\\_name@xxxxxxxx](mailto:my_name@xxxxxxxx)>
  - *Date:* Thu, 24 Jan 2008 01:09:28 +1300
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seegoon99@xxxxxxxx wrote:

On Jan 23, 1:21 pm, Terry Given <[my\\_n...@xxxxxxxx](mailto:my_n...@xxxxxxxx)> wrote:

seegoo...@xxxxxxxx wrote:

On Jan 23, 12:56 pm, Terry Given <[my\\_n...@xxxxxxxx](mailto:my_n...@xxxxxxxx)> wrote:

seegoo...@xxxxxxxx wrote:

Hi to all.  
I have been asked to look into a SMPS that is experiencing a higher than wanted failure rate in the field. Something that I've come across is ringing a bell.  
The controller chip (NCP1207) is driving a fet(IRFBE30) via a 47R resistor. The resistor is an 0805 smt package.  
Somewhere on this group in the past I've read something about gate resistors failing because they are under sized.(power wise)  
Is this possible in this case with such a small package.

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If the gate resistor goes high impedance it would obviously cause catastrophic failure of the FET and then surrounding components. Which is what we are seeing.

Could this be an issue?  
Cheers  
Rob

Hi Rob,

it certainly could be. if you look at the peak-pulse-power rating of 0805 resistors, you will see it isnt very good at all – the resistor comprises a very thin layer of resistive material atop a ceramic substrate, so there isnt much meat within which to dump the pulse energy.

the IRFBE30  $Q_g$  is about 60nC at 12V, so looks like about 5nF. at 47R thats 235ns time constant, which is a lot slower than the controller rise time. so the peak current is pretty much  $+12V/47R = 0.25A$ , and  $12V^2/47R = 3W$  peak pulse power.

thats not really very much; an 0805 can eat about 1W no problems, so I wouldnt expect this to be a problem. were the gate resistance more like 4R7, that would definitely ring alarm bells.

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part of the problem, of course, is that when the FET goes to the great silicon plant in the sky, it shorts D-G and then snots Rg and the controller.....making diagnosis that little bit trickier.

Panasonic make some AWESOME 0603, 0805, 1206 surge rated resistors (they make MMA0204 and MMB0207 look puny). although they are more expensive, they fit in the same footprint, and can be used to remove suspicion from Rg

BTW a 235ns gate time constant is pretty slow, and miller capacitance might be winning the fight against Rg, thereby stretching out the switching time even further, exacerbating switching losses. look at the gate waveform, at the plateau that occurs around Vth. This should be short (< 50ns). If it is not short, the gate drive is too weak. true for both turn on and turn off (although life is easy at turn-on for DCM).

if its a DCM smps, check it has a soft-start, as DCM supplies ALWAYS power up in CCM until the output cap is charged. A useful test is to set up some time delay relays to turn a unit on for, say 10s (enough for it to start running) then off for long enough for all the caps to discharge. repeat ad nauseum. this will pretty soon let you know if there is a start-up issue.

Cheers  
Terry- Hide quoted text -

Re: Gate drive resistor question.

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Hi there Terry.

There is something I forgot to add. There is a reverse diode across

the resistor to decrease turn off time. On turn on the Miller capacitance is definitely winning. In fact the gate voltage starts to

fall for about 2V , never mind level out!!

It seems that the gate resistor may well be a potential problem. I'm

going to see if I can increase it to a 2010 footprint.

As you have mentioned , once things have gone "pear shaped" it's

difficult to find the cause of the failure :0(

I'll check out if the supply has a decent soft start as well.

Thanks for the help.

Cheers

Robin

Hi Robin,

the diode halves the number of 3W pulses seen by the resistor, and in so doing halves the duty cycle, making life a bit easier for the resistor.

in that case, I'd definitely:

a) look at the panasonic parts (digikey has them) – easier than a PCB re-spin.

(an alternative would be to parallel 5 x 220R 0805, which will happily suck up 3W PPP ad infinitum.)

b) look carefully at the turn-on switching loss. if the gate drive is losing the fight with miller, the turn-on loss (if CCM) will be a lot higher than necessary. if its DCM, then the turn-on loss is  $0.5 * C_{stray} * V_{pk}^2 * F_{smpls}$ , regardless of switching time ( $C_{stray} = C_{ds} + C_{transformer} + C_{whateverelse}$ )

Cheers

Terry– Hide quoted text –

– Show quoted text –

Hi Terry.

I'll see if I can improve the turn on time. The fet is not getting to

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hot though. Even at full power (36W about) it's not getting much above 50deg c , so I'm not sure if it is that serious. There are some other changes that need to be made so a board redesign is probably on the cards anyway. I'm not sure I understand your turn-on loss equation. Is  $(0.5 * C_{stray} * V_{pk}^2 * F_{smpls})$  the power dissipated in the FET during switch-on? There is no reference to  $R_{ds}$  or current. I think I'm missing the boat here :0(

Cheers  
Rob.

Oh, OK.

if its DCM, then the current at turn-on is (by definition) zero. BUT when the FET turns on, the D-S capacitance (and xfmr capacitance and any other strays) have to be discharged, by the FET. so the FET dissipates  $0.5 * C_{total} * V_{pk}^2$  joules, each turn-on cycle – assuming the D-S cap was charged to  $V_{pk}$  just before the FET was switched on. so the power dissipation in the FET due to this ( $P = E * f$ ,  $1W = 1J/s$ ) is  $0.5 * C_{total} * V_{pk}^2 * F_{smpls}$ . usually (but not always)  $V_{pk} = V_{in}$

in CCM, in addition to this capacitive loss, there is  $0.5 * V_{pk} * I_{min} * T_{fall}$  energy dumped into FET, where  $I_{min}$  is the CCM current value at turn-on and  $T_{fall}$  is the drain voltage fall time – this assumes the FET current ramps up to  $I_{min}$  before  $V_{ds}$  begins to fall. so this switching loss is  $0.5 * V_{pk} * I_{min} * F_{smpls}$ . ditto for turn-off,  $0.5 * V_{pk} * I_{max} * F_{smpls} * T_{rise}$  (this last one is there in DCM too)

while the FET is on,  $R_{dson}$  comes into play, and you get  $I_{rms}^2 * R_{dson}$  conduction loss.

and just because the average FET temperature is 50C doesnt mean the junction is OK – ESPECIALLY during the turn-on (and turn-off) transients. Fairchild give thermal models for their FETs (eg FDP047AN08) use one of those and plug the swiching loss into it, you might be (unpleasantly) surprised at how high  $T_j$  can get in a short period of time – during switching edges, you can treat the IGBT die as if it were adiabatic, so all the switching energy causes the junction alone to heat, no heat flows into the tab. see "electro-thermal modelling of multi-megawatt power electronic applications using PSPICE" from [www.powerex.com](http://www.powerex.com)

Cheers  
Terry

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