

Re: Disobeying jet engines – why?

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On Jan 31, 1:43 am, Martin Brown <|||newspam...@xxxxxxxxxxxxxxxxxxxxxx>
wrote:
[...]

I challenge the ASM will do everything you need crowd to write a QUINE
(a program which when executed will output itself in sourcecode form) in
their favourite assembler language. I choose to do it in one line of
LISP.

Here you go in 8051:

```
ORG 0
..... Stuff deleted to save space
MOV DPTR,#0

LOOP:
LCALL DisasmDptr
MOV A,DPL
ORL A,DPH
JNZ LOOP
MOV PCON,#NAP_TIME
```

Other than the shown, all the code is from the library of stuff I have
already written.

```
((lambda (x) (list x (list 'quote x))))'(lambda (x) (list x (list 'quote  
x))))
```

It is among the shortest and a very old language dating back to the
60's.

Re: Disobeying jet engines – why?

Much is 'vague', for example if you use FPGA, then you depend on the vendor's soft to create the interconnects from the HDL.

This is a good point that a lot of people overlook. Even if you're programming in assembly, you're still making use of the (seemingly reasonable, at first blush) assumption that the code will execute the way you wrote it. With superscalar CPUs that dynamically reorder program execution, that's a HUGE amount of complexity going on behind the scenes to give the _appearance_ that that's what's happening, and of course the end result is that pretty much all "big iron" (32 or 64 bit desktop) CPUs today have non-negligible errata lists of what doesn't quite work the way it should.

The errata lists are surprisingly short considering how much clever stuff like register colouring and speculative execution is going on the background to keep the thing fully utilised at every clock cycle.

I remember when Cyrix commissioned a full formal proof for the design of an 8087 compatible chip their resulting validation suite found around a couple of dozen previously unknown defects in the Intel chip.

Regards,

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Martin Brown

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