

Part Time VLSI Design Engineering Certification Course from University of California and Cadence Design Systems

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Regarding the Certificate Program in VLSI Logic Design and Layout Design

Engineering.

TIIT (TTM Institute of Information Technology) in collaboration with the University Of California at Santa Cruz Extension in the Silicon Valley and Cadence Design Systems offers a certificate program in VLSI design engineering.

Students who complete the required courses with minimum grade point average

(GPA) will be awarded a certificate in VLSI design engineering (Physical

Design or Logic Design) from the University Of California Santa Cruz extension

in Silicon Valley.

Transfer your credits: After completion of the course you can transfer

12 Credits to your higher studies in USA with the University Of

California at Santa Cruz Extension in the Silicon Valley.

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You can also avail Scholarship

Course: Updated Exclusive courses for Layout Design & Logic Design Engineering.

Duration: Will be tentatively for 20 weeks.

Class Timings: Classes will be during the weekends; 6 (20 hours a day) days Lab will be open to work on Tools.

Placement Statistics: 90% of the people got employed in VLSI Industry so far.

Placement Assistance will be provided, and setting up mock interviews, resume building, seminar series etc will be provided.

Batches are Starting from : 15th March 2008

Hyderabad:

Prerequisites:

BE/BTech/ME/MTech/MSc in either computer science or Electrical/ Electronics

Registrations: Open Online @ http://tiit.in/registration_form.asp

Course contents:

You can see: <http://tiit.in/courses.html>.

Part Time VLSI Design Engineering Certification Course from University of California and Cadence Design Systems

- VLSI and ASIC Design, Introduction
- VLSI Engineering Fundamentals
- Introduction to IC Manufacturing (Visuals Included)
- Logic Synthesis Principles
- Advanced ASIC Physical Design
- Static Timing Analysis (Tools used: Common Timing Engine)
- System Integrity In SOC design (Tools used: Celtic for Xtalk, VSTORM for IR drop analysis)
- Seminars
- Demos of live design for all the tools.
- Verilog
- System Verilog
- Introduction to Formal Verification (LEC)
- Introduction unix/shell for VLSI Designers.

The following tools from Cadence will be used for the training:

- SOC Encounter XL, , Incisive Unified Simulator, RTL
- Compiler XL with BG and CTE, Virtuoso XL Layout Editor, Assura DRC/LVS,
- Assura RC, Virtuoso Schematic Entry.
- Celtic Cross Talk Analysis for Signal Integrity Analysis.
- VoltageStorm IR drop analysis Tools for Signal Integrity Analysis
- NanoRoute Global/Detail Router.
- verilog simulation– NCSim.
- Synthesis – RTL Compiler.

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- System Verilog – NCSIM.DFT – RTL Compiler.
- STA– CTE Engine.

Instructors: : Tools are taught by experienced working professionals.

Screening Test: You have to take screening test comprises of basic digital

electronics & Aptitude. Multiple–choice question.

Make sure: Since we will take only 20 Students per batch, we are getting

advance booking for Batches; make sure you will get the seat.

For more info:

www.tiit.in

www.time2mkt.com/training.html

www.cadence.co.in/support/university/ww_ustp.aspx

www.ucsc-extension.edu/ucsc/onsitetraining/vlsi.jsp

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Regards,

Priya

TIIT Hyderabad

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