

Re: CMOS for driving MOSFETS?

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- *From:* "Paul E. Schoen" <pstech@xxxxxxxx>
 - *Date:* Tue, 15 Apr 2008 00:33:05 -0400
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"Richard The Dreaded Libertarian" <null@xxxxxxxx> wrote in message <news:pan.2008.04.14.19.32.25.328974@xxxxxxxxxxxxxxxx>

On Sun, 13 Apr 2008 05:22:39 +0000, Jon Slaughter wrote:

"D from BC" <myrealaddress@xxxxxxxx> wrote in message

On Sun, 13 Apr 2008 04:56:30 GMT, "Jon Slaughter" <Jon_Slaughter@xxxxxxxx> wrote:

Why not use smaller mosfets to drive larger mosfet gates? One could put them in the same package so that logic level signals could be used to drive large mosfets? I'm thinking of implementing that idea discretely but maybe there is a reason for it? (although its going to cost me about 2x the # of transistors but its a clean switch)

I imagine that one probably could cascade cmos stages indefinitely to get very low gate drive requirements?

<http://server6.theimagehosting.com/image.php?img=CMOS-CAS.GIF>

The above is just an example, I use the same mosfets in each stage but the point is that each stage is easier to drive. (one might only need 1 or 2 stages for most fets).

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Is there any problem with this? (Besides the number of mosfets, but I imagine its no problem to do in silicon)

I suspect mosfet driver IC designers have thought of everything..

Example of one effort:

The IXDD414 mosfet driver functional diagram

<http://ixdev.ixys.com/DataSheet/99061.pdf>

shows a N and P FETs in the driver output stage.

Behind that, they're driven by gates (cmos again?)

A chain of cmos drivers might have an annoying propagation delay in some apps.

Hehe, well, thats one that uses one stage. I'm not sure what the propagation delay would be like but I'd imagine one wouldn't need more than 3 stages so it probably wouldn't be that big of an issue?

I think the point is more like, with the gate capacitance of the big mosfets, you need to be able to provide a pulse that will load the gate up with electrons, or suck them out as fast as possible, i.e., you have to provide a current spike – the more current your driver has available to charge/discharge that gate capacitance, the faster your big mosfet will switch.

However, it seems that there is also a characteristic rise and fall time that can be quite significant. I was surprised to find that the FQP90N08 has typical 360 nSec rise time and 160 nSec fall time. The HUF75645, with similar voltage, current, and RdsOn, switches in 117/97. And the IRFU3418, although rated at about half the current and twice the RdsOn, switches in 25/13 nSec.

Even more important than the gate capacitance to source may be the capacitance to source. When this is charged up at a high voltage, and the gate drive starts to turn the MOSFET on, the drain voltage starts dropping, which applies a negative current into the gate, tending to turn it off. This results in a "plateau", which keeps it in the dreaded linear region longer. But a good gate driver can be designed to have its best characteristic at this point. The TI drivers like the UCC27321 use a combination of MOSFETs and bipolar output drivers to deal with this Miller Effect.

Paul

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