

# HY57V643220CT datasheet

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## DESCRIPTION

The Hynix HY57V643220C is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V643220C is organized as 4banks of 524,288x32. HY57V643220C is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL. Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

HY57V643220CT datasheet:<http://www.chinaicmart.com/series-HY5/HY57V643220CT.html>