Re: Green solder mask and heatsinking

Source: http://sci.tech–archive.net/Archive/sci.electronics.design/2008–11/msg00144.html

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- *From*: krw <krw@xxxxxxxxxxxxxxxx>
- *Date*: Sun, 2 Nov 2008 08:14:03 –0600

In article <Mc7Pk.7948$Dm5.4636@xxxxxxxxxxxx>, unknown@xxxxxxxxxx
says...

> "krw" <krw@xxxxxxxxxxxxxxxx> wrote in message
> news:MPG.2376a9442301364598a365@xxxxxxxxxxxxxxxxxxxxxx
>
>> In article <wm5Pk.7938$Dm5.1486@xxxxxxxxxxxx>,
>> unknown@xxxxxxxxxx
>> says...
>>
>>> "Phil Hobbs"
>>> <pcdhSpamMeSenseless@xxxxxxxxxxxxxxxxxx> wrote in
>>> message
>>> news:490CD7E1.7080401@xxxxxxxxxxxxxxxxxxxxx
>>>
>>>> If you're solder–plating the copper anyway,
>>>> there's no reason not to
>>>> open
>>>> the solder mask––the cost is no different,
>>>> and the heat transfer will
>>>> be
>>>> very slightly better.
>>>
>>> Large areas of unetched copper is considered bad practice,
>>> especially
>>> with
>>> Mil–Spec, because of the differing thermal expansion
>>> between the copper
>>> laminate and the (typically fiberglass/epoxy) substrate. When
>>> large
>>> areas
>>> are needed because of shielding needs or a ground plane for a
>>> stripline,
>>> the
>>> etching pattern normally used is a grid or parallel traces
>>> which allow

> > > > for
> > > > thermal expansion without the copper lifting from the board
> > > > during
> > > > reflow.
> > > > Unfortunately this means the loss of surface area for heat
> > > > convection.

> > > Interesting. Large pours are "normal" in some neighborhoods (I've
> > > never done it) and certainly solid internal planes are the norm.
> > > How do they get away with the differential thermal expansion
> > > problem?

> > It depends on what you consider "large" is!

In the case of planes, the size of a panel is fairly normal.

> > I am generally talking about
> > areas around 35 x 35 mm, or about 2 square inches and up.

That's tiny to be a hard restriction.

> > It also depends
> > on just how reliable you want the board to be and whether rework or repair
> > is ever necessary. I suspect the modern designers are used to very fine
> > lines and more modern copper bonding technologies allowing them to ignore
> > differential thermal expansion. I do remember that most of the PCB CAD
> > programs I once used had the option of "cross hatching" large pours.

How is "cross hatching" any different? I'd think you still be
pulling at the corners of the "hatch". In any case, planes aren't
"hatched". I *have* seen boards that are somewhat balanced on
top/bottom (equal number of planes, etc) to reduce warping.

> > Microscopically, the copper foil contacting the substrate today is covered
> > with little "mushrooms" of copper grown electrolytically on the foil. When
> > used with a partially cured substrate (pre–preg), the high pressure curing
> > process locks the foil to the substrate quite tenaciously such that you
> > rarely see the copper lift from the substrate like you did 50 years ago.

50 years? No, I didn't see much of that 50 years ago either. ;–)
A *lot* of things have changed in 50 years.

> I still have some old printed circuit boards in the junque box where every through–hole is a small pad surrounded with a ring with only two small traces to connect the center pad and the ring. These are quite old and I suspect they were hand soldered.

Wasn't that to prevent delamination?

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Keith
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