Re: 90 degree bends in microstrip

Source: http://sci.tech−archive.net/Archive/sci.electronics.design/2009−03/msg01175.html

- *From*: John Larkin <jjlarkin@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx>
- *Date*: Sun, 08 Mar 2009 10:08:10 −0700

On Sun, 8 Mar 2009 09:34:11 −0700 (PDT), bill.sloman@xxxxxxxx wrote:

> On Mar 7, 8:26 pm, John Larkin
> <jjlar...@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx> wrote:
>
>> On Fri, 6 Mar 2009 13:48:46 −0800 (PST), makol...@xxxxxxxxx wrote:
>>
>>> On Mar 5, 8:34 pm, John Larkin
>>> <jjlar...@xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx> wrote:
>>>
>>>> On Fri, 6 Mar 2009 00:49:16 +0100, "Bill
>>>> Sloman"
>>>>
>>>> <bill.slo...@xxxxxxxx> wrote:
>>>>
>>>>> I was digging through some
>>>>> old reports from 1989 and
>>>>> found this text
>>>>>
>>>>> Microstrip Discontinuity
>>>>> Capacitances and
>>>>> Inductances
>>>>>
>>>>> A paper of this title was
>>>>> written by Peter Anders and
>>>>> Fritz Arndt
>>>>>
>>>>> and published in the IEEE
>>>>> Transactions on Microwave
>>>>> Theory and Techniques

MTT−28 (11) pages
1213−17 (November 1980).

Amongst other things it discusses 45 and 90 degree junctions in microstrips.

My reading of the conclusions is that

1. The problem is worst for 50R microstrip; the reflection

from a junction will be roughly at factor of three less from
the same junction in 75R track and another factor of three

down again for l00R track.

2. The reflection from a 45 degree junction is about a third of that
from

a 90 degree junction, so there is a small advantage in making a

90 degree change in direction as two 45 degree junctions.

3. The discontinuity can be reduced by about an order of magnitude by bevelling (they use the term mitering) the outside edge of the junction. For 90 degree junctions, the scale of the trim decreases with decreasing impedance, while for 45 degree junctions there in a smooth maximum in the trim around 75R.

Gigabit Logic's Application note 2 at Fig. 5, gives a figure of 1.8 times the track

width as the optimum length for the trimming cut for 90 degree junctions.

Applying the Anders and Arndt results, I get closer to 1.55 for a 50R track on PTFE,

1.77 for a 75R track, and about 2.2 for a l00R track, all for 90 degree junctions.

For 45 degree junctions in 50R track the equivalent figure is 0.91 of the width of the

track. For 75R track this increases to 1.5 of the track width, and for l00R track it goes

down a bit to 1.46 track widths.

Note that while our CAD system puts a radius on the outside corner of all track corners,

the area trimmed off by this feature is at least an order of magnitude less than that

removed by any of the trimming cuts specified above.

It is also worth noting that a via or a test pad inserted into a "constant impedance"

microstrip will introduce much larger reflections than an untrimmed 90 degree junction.

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The "trimming cut" is just
ths 45 degree cut off the
outside of the cormer −
for 90 degree

bends, and 22.5 degrees for
45 degree bends.

Below several GHz, risetimes above maybe
100 ps, square corners don't
matter.

John− Hide quoted text −

− Show quoted text −

correct.
everything in Bill's post may be true at 10 GHz but irrelevant below a
few GHz.

Mark

But at least he posted something about electronics, for which we can be grateful.

And John did express his gratitude with just the sort of graceful courtesy I've come to expect from him −

"Below several GHz, risetimes above maybe 100 ps, square corners don't
matter."

You expected gratitude? You believe in courtesy? Funny and funnier.

And all I stated in that post were facts. You find facts to be discourteous? Funnier yet.

In fact the whole point of the post was the reference to published paper on the subject

Microstrip Discontinuity Capacitances and Inductances
by Peter Anders and Fritz Arndt
IEEE Transactions on Microwave Theory and Techniques
MTT−28 (11) pages 1213−17 (November 1980).

and the salvaged text was thrown in to give an indication of the content. But John Larkin doesn't seem to read the electronics literature, and that aspect of the post would not have got his attention.

Your post didn't mention frequency at all. I wouldn't want people going to the trouble of clipping trace corners and worrying about vias when it makes no sense... which it usually doesn't. [1]

Right, I don't read all those 30−year−old old journals, but I do have a few pretty good books about such stuff. More important, I *do* occasionally add to my boards test traces and SMA connectors into power/ground planes, so I can measure capacitances and resistances and TDR things. That's reality.

Look:

ftp://jjlarkin.lmi.net/TDR1.jpg

ftp://jjlarkin.lmi.net/TDR2.jpg

On the TDR display, the junk at cm 2−3 is the SMA/pcb transition. The two right angles start at cm 4 and the capacitive bump at cm 5 is the via. On regular boards, right angles are down in the noise, buried in trace width variations and fiberglass weave.

This is on a scope with a 30 ps reflected TDR risetime. At 100 ps, things would be a lot flatter.

TDRing power pour/ground plane structures is fascinating. It blows away all sorts of popular dogma about planes and bypassing.

John

[1] Corner clipping is a legacy of hand−taped layouts anyhow; CAD makes nice smooth curves, which lots of olden−days layout people forbade because it contributed to tape creep.

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