

## Re: [Sci.nanotech] Re: End of lithography at 32 nm?

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Date: 30 Aug 2004 02:26:35 GMT

On 27 Aug 2004 16:39:39 GMT, erincss@aol.com (erincss) wrote:

>

>*well how far can micrometer chips built in three dimensions go, if done using  
>modern techniques?*

I don't think anybody has a workable 3D silicon IC process. Some high-density applications (flash memory, mostly) stack individual rectangular chips at right angles and wirebond in all directions, up to maybe 4 layers deep I think. This is OK if each chip is pre-tested (to keep yields up) and doesn't dissipate much power (because the stacking is terrible thermally.)

IC fabrication is pretty much planar, etching and implanting into the thin surface layer of monocrystalline silicon, then paving it over with vias and metalization layers. There's no good way to deposit more silicon and start a second active layer.

John